[54] COMPUTER CONTROL OF TELEVISION RECEIVER DISPLAY

[22] Filed: Dec. 30, 1976

[51] Int. Cl.2 .. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . G06F 3/14
[52] U.S. Cl. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 340/703; 340/723;
340/750; 358/93; 273/85 G
[58] Field of Search ..... 340/324 A, 324 AD, 152 R,
340/154, 747, 750, 703, 723; 358/93; 273/DIG.
28, 85 G

[56] References Cited
U.S. PATENT DOCUMENTS
3,829,095 8/1974 Baer ..... 340/324 AD
3,895,374 7/1975 Williams ..... 340/324 AD
3,928,845 12/1975 Clark ..... 340/324 AD
3,996,583 12/1976 Hutt et al. ..... 340/324 AD
4,052,719 10/1977 Hutt et al. ..... 340/152 R

Primary Examiner—Marshall M. Curtis
Attorney, Agent, or Firm—C. Michael Zimmerman

ABSTRACT

A method and apparatus for generating, under the con-
trol of a microprocessor, signals for operating a visual display mechanism of the scanning type. The position of the scan is tracked, and when it approaches a desired location on the display area for a particular segment to be displayed, it responds thereto by directing delivery to the scanning system of control signals which define the selected display segment. A plurality of display segments, each containing information at least partially defining one or more object images which may be desired to be included in a specified display, are stored in a cartridge memory which can also include specific operating instructions for carrying out a particular game or other function with such display segments. Each of the display composers includes an associative memory arrangement for addressing the cartridge memory and directing feedout therefrom of specified segments at times required during the scan. A FIFO buffer is also included in each of the display composers for delivering information defining an object image at a regular rate correlated to the scanning rate, irrespective of the time in which such information is made ready for the display.

22 Claims, 2 Drawing Figures
COMPUTER CONTROL OF TELEVISION RECEIVER DISPLAY

BACKGROUND OF THE INVENTION

This invention relates to the production of control signals for operating a visual display mechanism of the scanning type, such as a standard television receiver, and, more particularly, to a method and apparatus for inexpensively producing scanning control signals which provide a high resolution display and can be easily changed from display to display. The invention accomplishes this by composing under the control of a microprocessor each frame of a display substantially simultaneously with the time the display surface is being scanned to produce the same.

Until recently, standard television receivers of the type found in homes and places of congregation throughout the developed countries have been passive elements. That is, standard television receivers are used traditionally only to display programming transmitted to the same from an image pick up device, such as a camera. Television receiver control units are now available, however, which turn TV receivers themselves into active instrumentalities, i.e., instrumentalities in which the viewer can directly control or influence the actual display which is on the receiver screen at a given time. Such control units are typically designed for use of the television receiver as a game display, such as a display of a modified version of the game of ping-pong. The viewer becomes a participant in such a game by manipulating the screen display, which display may be programmed to react to the control in a particular way. For example, in the modified game of ping-pong the viewer or participant can move a paddle on the screen to intercept a ball. The ball will react to the interception by “bouncing” from the paddle with an appropriate deflection angle.

There are basically two different kinds of TV receiver control units of the game type. One is the so-called hard-wired type which includes specific logic designed to perform a particular function, such as play a particular game. Hard wired control units are quite limited in their use. That is, not only are such units limited to specific games, economics limits the same to quite simple games. Moreover, the amount of hardware required to provide a highly resolved visual display with multiple movements on TV receiver is more than what can be provided economically.

The other type of control unit now available utilizes a microprocessor as a primary component in order to gain the versatility inherent in such a device. Presently available ones, however, do not take full advantage of the resolution, color and movement capabilities of standard television receivers. For example, each frame of TV receivers built in accordance with the NTSC scanning standards adopted in the United States and Japan will be made up of 483 individual horizontal scan lines. Each scan line includes about 320 individual display points, each one of which can be individually defined. This means that on a standard 19 inch television screen, “dots” which are only about 47 mils apart, center-to-center, can be individually programmed to obtain good resolution.

The approach taken by most microprocessor-based control units now available is to duplicate or, in other words, “map” in a memory information defining a frame which is to be displayed, which information is then read out to the television receiver to control its display. It will be recognized that an inordinate and quite expensive amount of memory would be required to individually specify in the “map” different information for each one of the “dots” which individually can be generated by a TV scanning system. This is particularly true if a color display is generated. The information needed to specify each of the dots then must include color information, as well as intensity information. Because of this, it is the practice now to generate much larger, single color dots to make up a display, with the concomitant result that the resolution is likewise reduced.

The memory mapping concept now used to define the frames of a display results in another major limitation on presently available devices using microprocessors. Any appreciable object movement between frames requires that the content of the memory be altered, copied, exchanged or deleted. Thus, the step of moving an object in the display can be quite demanding on a microprocessor and is awkward to execute, particularly in the relatively short time, about 1.3 milliseconds, between fields.

SUMMARY OF THE INVENTION

The present invention provides methods and apparatuses for coupling a microprocessor to a scanning visual display apparatus which enables a highly resolved display to be obtained without inordinate memory requirements. It further enables display of complex object movements without straining the microprocessor. The invention accomplishes this by substituting for the present memory mapping concept now used in microprocessor-based controllers, the concept of composing substantially simultaneously with each scan the information which is to be conveyed during the scan. That is, it replaces the cumbersome concept of one-to-one correspondence of memory space to display space with a concept of time correspondence.

In accordance with the above, the invention broadly includes the method of composing each frame of the display substantially simultaneously with the scan which produces the same. The apparatus includes a memory which stores information sets, e.g., in the form of digital data, which define a plurality of spatial display segments for the display surface area which individually contain information at least partially defining an object image it may be desired to be displayed during a scan, and means providing information defining a background for object images to be displayed during a specified frame display. It further includes means which converts the display segment information and the background information to corresponding control signals for the scanning system. It also includes means which delivers the background defining information and the sets of spatial display segment information to the converting means at times during a scan of a specified frame display correlated with the desired spatial positioning during such scan of background and selected object images.

From the above it will be seen that each of the individual objects which may be displayed during the frame is stored and then addressed for delivery to the scanning system only as required to produce an image of the object in a desired spatial positioning. This is in contrast to prior arrangements which develop and store a map of an entire frame display. When display segments are not
being delivered to the scanning system, it is directed to produce a background desired for the display.

The aforesaid means which delivers information to the converter includes means which discharges information defining object images at a rate correlated with the rate at which the scanning system scans the display surface area. Preferably such means includes a first in-first out (FIFO) buffer which will discharge information at such a regular rate irrespective of variations in the regularity with which it receives such information.

The invention includes other features and advantages which will be described or will become apparent from the following detailed description of a preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWING
With reference to the accompanying two sheets of drawing:

FIG. 1 is an overall functional block diagram of a preferred embodiment of the apparatus of the invention illustrating the same connected between a television receiver and a processor; and

FIG. 2 is a detailed functional block diagram of a display composer of the preferred embodiment of the invention depicted in FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT
As mentioned previously, the invention replaces the cumbersome concept of one-to-one correspondence of memory to display space with a concept of time correspondence. That is, each of the frame displays is composed at the very time the frame display is being produced on the display surface area by the scanning system. In furtherance of this, each of the images of objects it may be desired to be displayed are provided in segments of display area, which segments are stored at predetermined locations within a memory. The scan producing a frame is then tracked, and on the scanning system approaching a desired location for a spatial segment having a desired object image, control signals conforming to the stored information defining the segment are delivered to the scanning system.

FIG. 1 illustrates a major block diagram of a preferred embodiment of the invention and the manner in which it is connected between a scanning display and a processing device. In this preferred arrangement, the scanning display is represented by a standard TV receiver 11; a digital to analog converter 12 which converts the digital scanning information delivered to it by the coupler of the invention to a composite video signal; and an RF carrier modulator 13 which superimposes a radio frequency carrier signal on the composite video signal to condition the same for direct application to the RF input (antenna input) of the TV receiver. The frequency of the carrier is changed to correspond to the bandwidth of an available channel in accordance with conventional practice. An input line 14 is included to represent such selection capability. The total scanning system is differentiated from the remainder of the system depicted in FIG. 1 by the dotted line enclosure 15.

The processing device in this preferred embodiment is a microprocessor having desired input and output active elements connected thereto. Such microprocessor is represented in FIG. 1 by the dotted line enclosure 16 and includes a central processing unit (CPU) 17 containing the arithmetic and control registers of the microprocessor and its logic, and a read-only memory (ROM) 18 for containing the operations program and subroutines for the CPU 17. The microprocessor could also include additional memory in, for example, the form of a RAM (a read and write memory) if desired for additional storage or manipulative flexibility. Although the invention can couple various general purpose microprocessors to a scanning system, a suitable one which is available and inexpensive is the one designated "F-8" produced both by Mostek Corporation, Carrollton, Texas, and the Fairchild Semiconductor Components Group of Fairchild Camera and Instrument Corporation, Mountain View, California.

The input/output instrumentalities of the processing unit are represented in FIG. 1 by block 19 and their nature will depend on the particular use to which the system is placed. For example, in game applications the input will include manipulative controls such as "joy sticks" and/or alpha-numeric keyboards enabling one or more players to direct movement of display objects on the TV receiver in accordance with playing of a game. The input will also include initiating mechanism, such as a manually operable coin-actuated OFF-ON switch. The output represented by block 19 includes all desired output from the system except for that to be displayed on the TV receiver 11. For example, during game play this output may include flashing lights, sounds, etc., to indicate reaching of a goal.

The CPU, ROM, and input/output blocks of the processing unit are connected together by a bus system 20 made up of an address bus 21, a data bus 22, and a control bus 23. This bus system will be referred to hereinafter as the microprocessor bus. The utilization of a bus concept makes it possible to add other microprocessor components as desired to increase the capability of the apparatus.

As one feature of the coupler of the invention, it appears to the CPU 17 as merely addressable memory, whereas when it is combined with digital to analog converter 12 and modulator 13 it appears to the TV receiver merely as an incoming video composite signal on an RF carrier. In this connection, the coupler is connected to microprocessor 16 basically only through the bus system 20 and it includes a display composite bus system 24. Bus system 24 is similar to system 20 in that it includes an address bus 25, a data bus 26 and a control bus 27. One or more display composers 29 which will be described in more detail hereinafter connect the bus system 24 to the scanning system 15. The display composers generate and provide to the scanning system 15 digital signals defining desired display picture information. Memory in the form of a ROM 31 also communicates with the bus system 24. Such memory provides sets of information in the form of digital data respectively defining a plurality of spatial display segments, each of which contains information defining object images it is expected to be desired to be displayed on the receiver 11. It further contains the programming necessary to define the specific game or other operations to be performed in connection with such display segments. For example, if the unit is to be used to play a modified sport game, such as a game of football or hockey, each of the players will be provided in the ROM 31 as one or more object images in spatial display segments. The programming provided by such ROM will include microprocessor instructions for playing the game.

From the hardware standpoint, the ROM 31 can be provided as a cartridge which plugs into the remainder
of the system. Different spatial display segments defining differing object images and specific operating instructions tailored thereon can be provided. That is, merely by replacing one ROM with another, the particular game or other function for which the microprocessor is coupled to the TV receiver can be changed.

The coupler of the invention includes a timing and sync signal generator 32 which develops and delivers to the digital to analog converter 12 the timing and synchronization signals required to produce a composite video signal for TV receiver 11. Such signals include all composite sync information, i.e., the directions required by the converter 12 to generate the synchronization and equalizing pulses required in a composite video signal, as well as color burst and color burst window information. The rate at which the generator 32 operates is controlled by the primary clock or timer of the coupler represented in FIG. 1 by block 33. The signals developed by generator 32 are delivered to digital-to-analog converter 12, as represented by flow line 34, to be added to the picture information also delivered to such converter by one or more of the display composers 29 as indicated by its input line 36.

Generator 32 also controls timing of the composition of displayed pictures by the display composers 29. In this connection, it delivers to such display composers the horizontal and vertical blanking signals which it also delivers to the converter 12. It also provides a bit rate clock for the output of the display composers. This flow of information to the display composers is represented in the flow diagram by the line 37 extending from the generator 32 to the control bus 28 of bus system 24.

Communication between the microprocessor bus system 20 and the display composer bus system 24 is controlled by a system controller enclosed within the dotted line block 38. Such system controller is basically comprised of two major components, interrupt logic represented at 39 and address and data latching registers represented by the block 41. The interrupt logic represented by block 39 provides control of communication between the bus systems 20 and 24, as well as intercommunication between components on the display composer bus system. The timing of the logic is correlated with the CPU timing. More specifically, timer 33 provides the CPU clock as represented by the flow line 42 extending between such timer and CPU 17. The logic timing is also controlled by the timer 34 as represented by flow line 43. As will be discussed hereinafter, line 43 also represents clock control by the interrupt logic.

Basically, only the microprocessor 16 (particularly the CPU 17 thereof) and each of the display composers 29 requests use of the address and data buses of either of the bus systems 20 and 24. In this connection, the CPU initiates communication not only with each of the other components of the microprocessor, but also with the display composers 29 and ROM 31 connected to the bus system 24. The display composers, on the other hand, initiate communication only with the ROM 31. In general, use of the address or data buses of either of the bus systems is given to the first requestor. If there is a conflict between a request made by the CPU and one of the display composers, the CPU has priority. Any conflicting requests made by different display composers is resolved by alternating cycles of use between the conflicting requestors.

The interrupt logic is designed to satisfy the following algorithm:

BUS CONTROL ALGORITHM

CPU Requests for Bus Use

The CPU can communicate through the bus system 20 with the microprocessor components connected thereto in a conventional manner. That is, it is only when the CPU wants to communicate with any of the components connected to the composer bus 24 that the system controller 38 is activated. As will become apparent hereinafter, at all times controller 38 is so activated if its first instruction is to the timer 33 to stop delivering clocking pulses on line 42 to the CPU during the transfer of information between the bus systems. This will prevent the CPU from reacting to address or data information in the process of being changed.

When interrupt logic 39 receives a request from CPU 17 for data contained in the cartridge ROM 31, such interrupt logic 39 will first instruct the timer 33 to discontinue sending clocking pulses to the CPU as discussed above. This has the effect of suspending operation of the microprocessor. When both the microprocessor bus system 26 and the composer bus system 24 are free (the immediately preceding grant cycle is finished), the interrupt logic 39 will gate the cartridge ROM address provided by the CPU on line 21 to address bus 26 of the composer bus system. Once such address is on bus 26, the logic will initiate a ROM reading cycle so that the data at such address will be fed by the ROM onto the data bus 27. At the end of a predetermined time interval selected to assure complete readout of data at any address of the ROM, the content of the data bus is gated into data latches in block 41 for subsequent delivery to the data bus 22 of the microprocessor bus system. The address and data buses of the bus system 24 are thereby freed for subsequent use. Simultaneously therewith, the interrupt logic directs the timer 33 to again deliver clock pulses to the CPU 17 to continue its sequence of operation.

As will become clearer from the later detailed description of one of the display composers, the CPU 17 transfers information into and out of such composers through memory registers and other memory locations. Each of the display composers has a distinctive selection address. When the CPU 17 initiates a request to read a memory location in a display composer so addressed, the request is made to the interrupt logic 39 through control bus 23 of bus system 20. The interrupt logic reacts to such a request by directing timer 33 to discontinue sending clocking pulses to the CPU, with the result that further execution of instructions by the CPU will be suspended. At the earliest time the address and data buses of the composer bus system 24 is free, the interrupt logic will gate the composer address desired from the address bus 21 through an address latch of registers 41 to the address bus 26 of the composer bus system 24.

When CPU 17 initiates a request to enter information into a memory location of one of the display composers 29, its request is applied to the control bus 23 and is received by the interrupt logic 39. The interrupt logic again initially reacts to a request from the CPU for use of the bus system 24 by directing timer 33 to discontinue sending clocking pulses to such CPU in order to suspend its operation. At the earliest time the bus system 24 is free, the interrupt logic will direct gating to address bus 26 through an address latch of registers 41 of the address present on bus 21 it is desired information be
entered. Such logic will also indicate which display composer is being addressed. The selected composer will react to the address by entering into the addressed memory location the information then on data bus 27. At the end of a preselected write time cycle, the composer will pulse the interrupt logic to indicate that it has received the address data. The interrupt logic will react thereto by directing timer 33 to again deliver clocking pulses to the CPU so that its operation is restarted.

Frame Composer Requests for Bus Use

As mentioned previously, initiation of reading of information from the ROM 31 by any one of the display composers 29 is also controlled by the interrupt logic 39. When one of such display composers desires data from the ROM, the interrupt logic 39 reacts to a request for such data on the control bus 28 by permitting the particular display composer to read out the desired ROM address onto the address bus 26. The interrupt logic further initiates a read-out cycle from the ROM and directs the display composer to gate in such data. At the end of the preselected period, the interrupt logic is strobed to indicate that the bus system 24 is free for other use.

FRAME COMPOSERS

The frame or display composers 29 are a major component of the present invention. They compose the control signals for each frame to be displayed substantially simultaneously with the display of such frame. The composers accomplish this function by selecting which of the display area each spatial segment containing a desired object image is to be shown during a frame; reading from ROM and delivering to the scanning system 15 information defining each spatial segment as it is required during a scan; and producing and delivering to the scanning system background control signals at all other times during a frame scan. In this connection, it should be noted that an object image contained in a spatial segment stored in the ROM 31 is not necessarily an image of a full object when it is displayed on the screen of receiver 11. For example, the object image in a selected spatial segment could be an image of a leg of a football player at a particular orientation, e.g., kicking a football, which will be displayed with another spatial segment from the ROM providing the body of the player. A ROM spatial segment can also include two or more separately identifiable images, such as that of a projectile hitting a tank. The ROM spatial segment can also be one which requires another spatial segment to be superimposed thereon before an identifiable object image is provided, e.g., one spatial segment could define green pants and helmet for a football player while another could define a red jersey for such player. Thus when it is stated a spatial display segment having an object image is stored in the ROM 31, it is meant that information is stored in such ROM which can be manipulated by a frame composer to produce the control signals for the scanning system necessary to compose a preselected spatial display on the TV receiver 11 having dimensions significantly less than those of the full display area of the receiver. Each of such display segments typically includes information at least partially defining an object image. In the particular implementation of the concept of the invention provided by the preferred embodiment being described, each of such spatial display segments is rectangular and often includes information defining background surrounding the object image.

It should be noted in connection with the following that each television raster scan or, in other words, frame is made up of two interlaced fields, an odd and an even field. Thus, whenever hereinafter reference is made to "a field display", one of the fields of a television frame display is being discussed.

Each of the frame composers 29 is capable in this preferred embodiment of directing the display of 16 different spatial segments during each television frame display. Thus when it is expected that more than 16 segments may be displayed during one frame, such as during a modified football game between two eleven-man teams (one man per segment), a sufficient number of frame composers can be applied to the composer bus 24 to accommodate all of such segments. Moreover, separate frame composers are used in this preferred embodiment to superimpose one segment on another during a raster scan. It will be recognized that the number of frame composers which can be included in an embodiment of the invention is not limited except by the processing and communication capability of the particular embodiment.

FIG. 2 is a functional block diagram of a preferred frame composer for the invention. The spatial position nomenclature used therein is based on Cartesian coordinates with "X" representing the direction of each scan line and "Y" the direction orthogonal to the scan lines. Each dot on a scan line represents a count of one in the X direction, and each scan line represents a count of one in the Y direction.

Each frame composer includes an address decoder 51 which intercepts all requests to address any of the registers or memory locations to be described. In this connection, the address decoder input is connected to the address bus 26 of the bus system 24, and the decoder is provided with a multiplicity of ENABLE outputs which are individually connected (not shown) to the various registers and memory locations of the frame composer. Each frame composer further includes a command register 52 which not only enables or disables the entire frame composer as an entity, it also enables or selects various function within the frame composer as will be described. It is loaded from the data bus 27 of bus system 24 under the control of the CPU 17.

Each composer of the invention includes means for delivering background defining information and sets of information defining the spatial display segments to the scanning system. Such means includes an associative memory arrangement for listing the spatial display segments to be shown during any specified frame display and the spatial location desired for each in such display. It should be noted that a determination of a desired spatial location for a segment is also a determination of when the segment is to be displayed during the scanning operation for the frame. Information defining a location desired for a segment on the display surface area thus can be referred to as "time-distance" information. The associative memory arrangement also lists the attributes, such as color and intensity, the object images are to have in the specified frame display.

The associative memory includes a pair of CAMs (content addressable memories) 53 and 54, as well as a RAM memory 56 which is operatively associated with each CAM. The CAMs list the spatial segments in accordance with their order of appearance in the X direction, i.e., the order of their X values. That is, dur-
ing any specified frame, one of the CAMs lists all of the spatial segments to be displayed in the order in which such segments will be required by the scanning system during the frame scan, irrespective of the location of such segments in the Y direction. While the segments are listed in the order of their appearance in the X direction, it is the line on which each of the segments first appears during a scan or, in other words, its "Y value" which is actually contained in the CAM. As an example, with reference to CAM 53 (list A) it will be seen that the X order of the spatial segments to appear in the frame display represented by CAM 53 have, in order, the Y values of 65, 50 . . . 84. While each of the CAMs has a memory size enabling the listing of 16 different spatial segments, only three, the first two and the last one, are illustrated in FIG. 2. As will be described more fully below, each of the CAMs 53 and 54 is to be used alternatively depending on whether or not there is a change in the X order of the segments between discrete frame displays.

RAM 56 also provides a list accommodating 16 different spatial segments. While the segment entries in the RAM list are not in any particular order, each is distinctively associated with its Y value in the CAM being used at the time. The RAM listing for each of the spatial segments includes the number of scanning lines that have information defining the particular spatial segment (delta Y), the location along each of the lines first encountered by the scanning system which includes information on the spatial segment (its X value); the length in bytes of the segment along each of the lines (delta X); the address in the ROM 31 at any given time giving the location of the segment information which will be required next (the ROM pointer); and the attributes, e.g. color and intensity, desired for the object image or images in the segment. The list in the RAM further includes for each of the spatial segments an "X copy" bit which will be explained hereafter.

Means are included for tracking the scan of the scanning system as it produces each frame display. That is, a line counter 57 is included which keeps track of the position of the scanning system in the line or "Y" direction by counting the lines scanned during each field. Counter 57 is reset by the vertical retrace pulse of the timing signal as indicated by the V-blank input 58 to a line advance skew 59. Skew 59 is included to advance by one the count being registered by counter 57. It has been found that such a one-line advance provides the composer with the least time it requires to assure that information required for scanning is at its output when needed by the scanning system. In this connection, in one actual embodiment each scanning line is scribed in about 64 microseconds. Thus, the line advance provides a 64 microsecond advance to the operation of the composer.

Line counter 57 acts as a comparand register for whichever of the CAMs 53 and 54 is in operation during scanning for a particular frame. Its value is incremented by one for each scanning line during the horizontal retrace for the next line to be scanned. Such counter cooperates with a display control 61 to direct delivery to a first in-first out (FIFO) buffer 62, digital information defining the upcoming line to be scanned. That is, assuming subtractor 63 (the purpose of which will be discussed hereinafter) is not actuated at the time, the value registered by line counter 57 will be simultaneously compared at the beginning of each horizontal retrace with all of the Y values listed in the particular CAM which is to be compared therewith during a specified frame as determined by selection logic 64. As an example, if line counter 57 is registering the count "65" and it is compared with the list in CAM 53, a favorable comparison will be registered for the spatial segment denoted "1". This will result in the hit register 66 issuing a "hit" signal to the display control 61. Hit register 66 has additional activating input from the RAM 56. That is, it continues to issue hit signals to the display control 61 for any of the spatial segments which were first displayed on earlier scan lines during the frame but have a length in the Y direction which requires information defining the same to also be displayed on the particular scan line being loaded into the buffer 62. This is represented by the flow line 67 extending to such register from the delta Y portion of RAM 56. In the particular example being used, the RAM 56 will indicate to the hit register 66 that segment II is also to be displayed on scan line 65. That is, such segment first appeared on line 50 as is evidenced by the Y value for the same located in CAM 53. Its length in the Y direction, however, is twenty lines, as indicated in the delta Y portion of the RAM, with the result that information defining the segment also appears on scan line 65. It should be noted that the delta Y of each segment which has appeared on a line is decremented before the start of the next line so that the delta Y for such segments will become exhausted and not provide input to hit register 66 when information defining the segment is no longer to be part of a scan line.

Upon receiving a hit signal from register 66, display control 61 will respond thereto by initiating several operations. It will first direct RAM 56 to deliver through an offset adder 60 (the purpose of which will be brought out later) to an adder/subtractor 68 the X value of the first spatial segment to be displayed on the line in question. The adder/subtractor will utilize such information along with the horizontal scanning pulse to calculate the length of background at the beginning of the line prior to the first spatial segment to be displayed on the line. This background length or, in other words, time-distance information will be delivered to an information section 69 of the FIFO buffer in numeric form as represented by flow line 70. In the example being used, the adder/subtractor 68 will deliver the number "39" in binary form to the section 69 since there are 39 dots of background which are to be produced in the specified frame prior to the appearance of the first spatial segment, segment I. The display control 61 will also deliver to an indication section 71 of the FIFO buffer a symbolic bit (in the example, an "O") which indicates that the information delivered to section 69 by the adder/subtractor is background information. This is represented by the flow line 72 extending from the display to such buffer section.

Once the information defining the initial background, if any, is delivered to FIFO buffer 62, the information required by such buffer to display the first spatial segment appearing line the line is then loaded. More particularly, display control 61 directs RAM 56 to deliver to the attribute section 73 of the buffer 62 the digital information in such RAM defining the color and color intensity the object image or images within the first segment are to have during the frame display. RAM 56 also delivers a segment indicator (a "1" in the case of the example) to FIFO buffer section 71.

The segment indicator is also sensed by direct memory access (DMA) logic set apart by dotted line outline
74. Such sensing is represented by information flow line 76. DMA logic 74 acts, in effect, as means responsive to the scan tracking indicating that the scanning system is approaching a desired spatial position for a selected spatial segment by directing the ROM to deliver information required to produce such segment to the information discharging portion of the composer. Logic 74 also acts to update those variables in RAM 56 which are decremented or incremented for a display.

DMA logic 74 includes an image addresser 77 which takes from the ROM pointer section of the RAM 56, the ROM address for the first information defining that portion of the segment which is to appear on the line being scanned and delivers it via the address bus to the cartridge ROM 31. The cartridge ROM reacts thereto by delivering the information at such address for the line being scanned to the information section 69 of the buffer 62 as is represented by flow line 78. In this connection, the information defining a segment is stored in the ROM as symbolic digital data in one byte sections, one at each address. The DMA logic therefore includes a delta X decrement 79 which reacts to the number of bytes defining the segment in the X direction by advancing the image addresser from one address to another until such time as the number of bytes of information required to define the spatial segment on the line is delivered to the buffer 62. Once the information is so delivered, the address specified for the segment in the RAM 56 is updated to the address which provides the first information required for the next line of the segment to be produced. This is represented by flow line 81 extending to the ROM pointer portion of the RAM 56 from a RAM values update block 82 within the DMA logic 74. The delta Y for the segment is also decremented by the DMA logic at this time for the purpose discussed earlier. Such decrementation is represented by the flow line 83 extending from the update block 82 to the delta Y portion of the RAM 56.

In the particular example being used in which the spatial display segment labelled "I" follows the first background information, image color and intensity indicia "10100" will have been delivered to attribute section 73 of buffer 62, the binary bit "1" will be delivered to the indicator section, and the binary data "00001101" defining the segment will have been delivered to the information section of such buffer. In this connection, it should be noted that the information set defining the segment includes information defining the background for object images within the segment. In this example, a binary "0" represents a background dot whereas a binary "1" defines an object image.

After the information required to display spatial segment I at the proper location is loaded into buffer 62, information defining the background, if any, between it and the next segment in sequence is loaded into the buffer. To this end, display control 61 directs that the X value of the next segment be delivered to adder/subtractor 68 along with the delta X value from the segment just loaded. Adder/subtractor 68 calculates from such information the time-distance or, in other words, length between the segments which are to be sequentially displayed, and delivers the result of such calculation to the information section 69 of FIFO buffer 62. In the example being used, such length is 27 dots, the difference between the end of spatial segment I and the beginning of spatial segment II. Again, this information is provided to the information section in numeric form, and the display control delivers to the indication section 71 a symbolic bit which indicates that the number represents background information rather than spatial segment data.

Information defining spatial segment II can then be delivered to buffer 62 in accordance with the procedure discussed above in connection with segment I. Additional background and segments to complete the line will sequentially be delivered to the buffer. In this connection, the time-distance or length for the last background in the line is calculated by the adder/subtractor 68 from the delta X of the previous segment and the horizontal retrace pulse at the end of the line.

This sequential operation of delivering to the buffer 62 all of the information needed by it to define a line can be completed in a relatively short time. In this connection, the information required for most scans of a line easily can be completed during the horizontal retrace time. However, depending on the depth of the FIFO buffer, more complicated displays may require the information delivery to be completed after the actual scan of the line has started. The provision of a FIFO buffer 62 as part of the information discharge means prevents such a delay from affecting the operation of the scan system. More particularly, it is only necessary that the information be delivered to the buffer prior to the time it is actually required during the scan since a FIFO buffer will immediately deliver to its output any information which is received by it.

The information discharge means of which the buffer 62 is a part is contained within the dotted line section 84. Such discharge means assures that the information defining a line being scanned will be delivered to the scanning system at a regular rate correlated with the rate at which such scanning system scans the display surface area of the TV receiver to produce a frame display. More particularly, the buffer 62 delivers the background defining information to selection logic 86 whose output is correlated with the bit rate and which delivers the symbolic information defining the individual segments serially at such rate. Control of the rate of the discharge from buffer 62 of the segment information is represented by bit rate clock input 87 to such buffer, and control of the rate at which background information is delivered to the scanning system is represented by a similar input 88 to selection logic 86.

At the beginning of a line scan, the first information delivered from buffer 62 will be the information defining the length of background before spatial segment I is displayed. That is, the selection logic 86 will first decode the background length numeral and cause delivery to the scanning system of background information for the number of dots so designated. The background information for the display surface area is provided by a background color and intensity register 89 which is loaded via the data bus 27 under the control of the CPU. Immediately after such delivery of the first designated background information is finished, the buffer 62 will serially deliver to logic 86 both the data defining the spatial segment I and, when required, the color and intensity information for the object image or images therein. When the spatial segment data indicates background, the selection logic will direct register 89 to deliver information defining the same to the scanning system, whereas when the segment data indicates an object image, the selection logic 86 will direct to the scanning system the color and intensity information for the spatial segment contained in the attribute section 73 of the buffer.
The discharge arrangement will continue to serially direct to the scanning system information defining the line being scanned until such time as the line is finished. The entire process will then be repeated for the next line. In this connection, when a field for a frame display is completed in accordance with the above, the line counter 57 will be reset by the vertical blank pulse and those values relating to spatial segments which have been changed during the field scan will be updated. That is, the delta Y's of the segments which have been displayed will be updated to their full value and the ROM pointer address of each displayed segment will be updated to that address in the ROM which contains the first information which will be required for the segment in question during the next field.

The delta Y and ROM pointer addresses will be similarly updated between frame displays. Moreover, if there is a difference in the X order of the segments to be displayed, command register 52 will issue a selection bit to CAM selection logic 64 to change the CAM list which is compared during the frame scans. In this connection, providing a pair of CAMs enables the X order set forth in one to be updated during a display while the other is being used for comparisons.

The simultaneous composition of a display at basically the same time the display is produced by a scanning system provides significant versatility to the kinds of information which can be displayed. Moreover, it enables manipulations and other functions related to the display to be carried out in relatively straight-forward manners. The preferred embodiment of the invention being described includes arrangements for performing certain functions and manipulations relating to the display which are especially desirable. For example, with the instant invention it is a simple matter to "zoom" or, in other words, enlarge or contract the spatial segments which are displayed. To this end, the apparatus includes memory means in the form of a zoom register 91 which stores information it receives from the data bus 27 defining a size multiplication desired for a spatial display segment. As illustrated, the zoom register 91 communicates with the output of the selection logic 86 represented by flow line 92. Upon receiving an enabling command from control register 52, the zoom register 91 will deliver the multiplication information to logic not shown) at the output which will multiply the spatial segment data accordingly to enlarge the segment as displayed.

The apparatus of the invention also includes an arrangement for modifying the color and/or intensity information emanating from the selection logic 86. More particularly, a color and intensity modifier register 93 is provided to store color and intensity information which is exclusively OR'ED, as represented by gate 94, with the display color and intensity information prior to its delivery to the scanning system. Thus, the color or intensity of either the object images or the background can be changed as desired. In this connection, it may be desired to change the same between sequential frame displays or sets of frame displays in order to present to the viewer a flashing color display.

The composer also includes means which will cause a display segment to be repeatedly displayed. More particularly, the "X copy" of RAM 56 is for the purpose of containing a symbolic bit of information associated with each of the segments indicating whether such segment is to be repeated when it is addressed. If it is to be so repeated, the bit of information is conveyed to the image addresser 77 of the DMA logic to direct the same to not be decremented during a line scan but rather to repeat the address contained within the ROM pointer section of such RAM until such time as the delta X for the segment is exhausted. The RAM value update 82 will then update the ROM pointer to the address for information appearing on the next scan line, which address will again be repeated during the succeeding line scan for the number of times indicated by the delta X decrement. Thus the information delivered from the cartridge ROM 51 to the spatial segment data section 69 of the buffer 62 during each line scan will be repeated so the scanning system will produce the selected segment a plurality of times adjacent one another on the display surface area. This function of the apparatus is particularly useful in producing a repetitive background on the display area, such as a checkerboard background.

The coupler of the invention also includes means enabling the display provided by the composer to be limited to a specified portion of the full display surface area rather than fill the same. This aspect of the invention is useful, for example, in a game in which it is desired to simultaneously present two different displays on a single TV receiver, each of such displays filling a separate half of the receiver. The different displays would then be composed of separate composers, each one of which would limit its display to the half of the display surface area assigned to it. Offset arrangements for both the X and Y display directions provide this display limiting function. Insofar as the Y direction is concerned, the offset arrangement includes a Y offset register 96 for storing information indicative of the location in the Y direction on the display surface area that the first line to be scanned is to be positioned. Offset subtractor 63 responds to the offset register 96 containing information indicative of a starting location for the first line different than the normal starting line, i.e., a line count different than zero, by delaying the start of the comparisons by the hit register 66 until such time as the line counter 57 reaches the count indicated by register 96. The subtractor further disables the output of the background register 89 until the offset count is reached, as indicated by disable flow line 97. The display in the Y direction will therefore not start until such time as the Y offset register count is reached. This will prevent the picture information from the composer from being displayed in that portion of the display area above the Y offset register count. It will be recognized that if it is desired to prevent a display below a particular location, the display can be so limited by disabling the background register when a count set forth in the Y offset register is reached.

An X offset register 98 is provided as an input to the offset adder 60 to enable the display to be limited in the X direction. Whatever count is contained in the register 98 will be added by adder 60 to the X value delivered from RAM 56 to the adder/subtractor 68. This will offset the scan in the X direction by the number of dot counts indicated in the X offset register and, hence, limit the display to the righthand portion of the display area. If it is desired to limit the display to the lefthand portion of the display area, the count in X offset register 98 can be used to inhibit the output of the discharge means 84 on each line after the count is reached.

The apparatus enables an interrupt signal to be generated for application to the CPU interrupt pin at any designated scan line. To this end, it includes a Y interrupt register 101 which receives from the data bus 27.
under control of the CPU 17 information designating a
line at which the interrupt signal is desired to be issued
during a given frame display. Upon receiving an en-
abling command from command register 52, a compara-
tor gate 102 compares the value in Y-interrupt register
101 with the count of counter 57. Upon comparison of
equality, gate 102 will issue an interrupt signal for appli-
cation to the CPU interrupt pin as represented by flow
line 103. The CPU can react thereto in any desired way
determined by the programming, such as by shifting
from one set of instructions to another.
In some games and other potential applications of the
apparatus of the invention, it is desirable to be able to
store a location on the display area being scanned at a
particular time when an external command signal is
received. For example, in a war game it may be desir-
able to be able to point or "shoot at" a location on the
display surface with a light pen or the like to indicate a
"hit" at such location. A simple means for storing or, in
other words, freezing such a location is also included in
the preferred embodiment. To this end, the composer
includes a dot counter 104 in addition to the line counter
57. Whereas line counter 57 keeps track of the line being
scanned at any given time dot counter 104 keeps track of
the dot or location in the X direction along each line
as it is being scanned. In this connection, dot counter
104 resets input as represented by flow line 106
from the horizontal retrace signal.
After receiving a freeze ENABLE signal from com-
mand register 52, both line counter 57 and dot counter
104 will dump respectively into Y freeze and X freeze
registers 107 and 108 their values on receiving external
stimuli as represented by the "freeze" flow lines 109.
The content of the freeze registers 107 and 108 can be
interrogated by the CPU to initiate an action based on
the values therein. For example, if the external stimuli is
provided by a light pen acting as a gun in the manner set
forth earlier, the action initiated by the CPU may be the
presentation of a spatial display segment in the next
frame showing as an object image an explosion at the
frozen location.

SYSTEM PROGRAMMING

As mentioned previously, all of the registers and
other memory locations within each of the composers
45 is accessed by the CPU through the address decoder
of the particular composer in question. Addressing of the
delta Y, ROM pointer and image color and intensity
sections of the RAM should be avoided during the time
such values are being updated between fields or frames.
Also spatial segments should be written into the CAM
and RAM only during the vertical blank between even
and odd fields. Otherwise, the composers are freely
addressable subject to the availability of bus system 24.
As discussed earlier, for each composer there are 16
potential objects that can be displayed, and hence the
RAM 56 and each CAM 53 and 54 are 16 entries long.
Any entry in a CAM list that is within the range of
actual Y (line) values visible on the screen will be inter-
preted as a segment to be displayed on the screen. For
NTSC systems this range is 0-263 lines. Thus, if fewer
than 16 objects are being displayed at a given time, some
of the CAM entries contain values outside of the
appropriate range; this in effect disables that entry.
In one specific implementation of the invention, the
65 registers in each display composer are classified into
three categories; WRITE ONLY, READ ONLY and
READ_WRITE. The WRITE ONLY and READ
ONLY registers perform mainly control and status
functions. The READ_WRITE registers are used to
describe the segments being displayed. All of these
registers are accessed by the CPU 17 through its memo-
ry address space. When accessing composer registers in
such implementation, the following rules should be ob-
erved:

(1) Avoid accessing composer registers during the
direct memory access logic window which occurs dur-
ing the first two H-blank pulses (lines 0 and 1) following
the leading edge of V-blank.

(2) Adding a new segment of the screen (or at least
placing it on the active CAM and RAM list) should
only be done during the V-blank between even-to-odd
field transition (excluding DMA window time). This
also applies to control bits of the command register.

(3) The optimal time to move a segment on the dis-
play area by switching from one CAM list to the other
and changing the X value of the segment if necessary is
during lines 3 to 21 of either field.

| Display Computer Address Assignments - Specific Implementation |
|---|---|---|---|---|---|---|---|
| Write Only Registers: | ADDRESS |
| Command Register | 11111011 |
| Zoom Register | 11111010 |
| Background Register | 11111010 |
| X-Off Register | 11111001 |
| Y-Off Register | 11111000 |
| Final Modifier Register | 11111000 |
| X-Interupt Register | 11111000 |
| Read Only Registers: | ADDRESS |
| X-Freeze Register | 11111000 |
| Y-Freeze Low Order Register | 11111000 |
| Y-Freeze High Order Register | 11111010 |
| Current Y Low Order Register | 11111010 |
| Write/Read Registers: | ADDRESS |
| Associate Memory: | 0000XX |
| ROM Pointer Low Order | 0000XX |
| ROM Pointer High Order | 0000XX |
| and Color | 0000XX |
| 4X, Intensity & X-Copy | 0010XX |
| AY Register | 0011XX |
| X Value Register | 0100XX |
| Y Value Low Order List A | 0101XX |
| Y Value Low Order List B | 0001XX |
| Y Value High Order and X | 011XX |
| Order List A | 011XX |
| Y Value High Order and X | 000XX |
| Order List B | 000XX |
| Write Only Registers: | Address = F7 |

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>INT.</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>N.O.</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A/B</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Y-ZM</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEL.</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FRZ</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENB</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INT.</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEL.</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FRZ</td>
<td>0/1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FRZ: Freeze bit defines CPV Interrupt Pin as an input
(FRZ=1) such that when it is stimulated externally,
the contents of the Dot Counter and Line Counter
are instantaneously copied into the freeze registers
which can be interrogated by the CPU.
ENB: Enable bit, 0=all DMA, Video and X logic activi-
ties of composer are disabled. 1=composer is en-
abled.
INT: Interrupt bit, this bit only has affect when the
FRZ bit equals 0. In this case, the Interrupt pin is
defined as an output.
INT=0=interupt disabled
INT=1=interrupt enabled, and interrupt source is
defined by INT. SEL. bit.
INT. SEL.: When FRZ=0 and INT=1, this bit selects the
interrupt source
INT SEL = 0 = V-blank is interrupt source
INT SEL = 1 = Y counter compare with Y interrupt
register is the interrupt source.

Y-ZM: Y-Zoom bit
Y-ZM = 0 = no room in Y direction
Y-ZM = 1 = zoom in Y direction as indicated by Y-
multiplier.

X-ZM is arranged to be on at all times.

A/B: Specifies which list, A or B is to be used by X and
CAM logic.
A/B = 0 = B list active
A/B = 1 = A list active

YINT H.O.: This is the high order bit of the Y-Interrupt
Register.

Zoom Register - Address = F6

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>X2</td>
<td>X1</td>
<td>Y10</td>
<td>Y1</td>
<td>Y2</td>
<td>Y1</td>
<td>Y0</td>
<td></td>
</tr>
</tbody>
</table>

X-MULTIPLIER: Y-MULTIPLIER

| 0000 = No multiplication (x1) |
| 0001 = x2 |
| 0010 = x4 |
| 0100 = x8 |
| 1000 = x16 |

X-MULTIPLIER:

| 0000 = No mult. (x1) |
| 0001 = x2 |
| 0010 = x4 |
| 0100 = x8 |
| 1000 = x16 |

Background Register - Address = F5

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>X2</td>
<td>INT 1</td>
<td>INT 0</td>
<td>BLU</td>
<td>GRN</td>
<td>RED</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This register specifies the color and intensity of the
screen background. INT 1 and INT 0 are the inten-
sity bits to be interpreted as follows:

<table>
<thead>
<tr>
<th>INT 1</th>
<th>INT 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Lowest Intensity

Highest Intensity

RED, BLUE and GREEN are the color bits, present-
ing eight possible colors:

<table>
<thead>
<tr>
<th>RED</th>
<th>GREEN</th>
<th>BLUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Black</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Blue</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Green</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Green-Blue</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Red</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Red-Blue</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Red-Green</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>White</td>
</tr>
</tbody>
</table>

Y-Offset Register - Address = F4

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>Y7</td>
<td>Y6</td>
<td>Y5</td>
<td>Y4</td>
<td>Y3</td>
<td>Y2</td>
<td>Y1</td>
<td>Y0</td>
</tr>
</tbody>
</table>

MSB = Most significant bit
LSB = Least significant bit

This register specifies a fixed offset for the Y co-
ordinates of all segments to be displayed. In affect it de-
dines where line Y = 0 is located on the display area. If

this register = 0 then line 0 is the first line immediately
following the rising edge of V-blank.

X-Offset Register - Address = F3

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>X7</td>
<td>X6</td>
<td>X5</td>
<td>X4</td>
<td>X3</td>
<td>X2</td>
<td>X1</td>
<td>LSB</td>
</tr>
</tbody>
</table>

X8 | Y8 |

Specifies the amount of offset from the left side of the
screen if X-Offset = 0 then X bit position occurs at the
first bit clock after the trailing edge of H-blank.

Final Modifier Register - Address = F2

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>INT 1</td>
<td>INT 0</td>
<td>BLUE</td>
<td>GRN</td>
<td>RED</td>
<td></td>
</tr>
</tbody>
</table>

The final video output pins are always exclusive OR'd
with the contents of this register.

Y-Interrupt Register - Address = F0

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

This registers contents (plus the Y INT H.O. bit in the
Command Register) are compared with the current
line counter contents and if the INT. bit = 1 and INT
SEL bit = 1 then a true comparison will result in a
lower voltage state being placed on the CPU inter-
rupt pin.

Read Only Registers

X-Register - Address = F8

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

This register receives a copy of the current dot counter
(the current X co-ordinate of the scanning beam)
when the FRZ bit = 1 and a negative transition is
detected on the CPU interrupt pin.

Y-Freeze Low Order Register - Address = F9

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>-1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

Receives a copy of the current Y-counter (current line
number) when the FRZ bit = 1 and a negative transi-
tion is detected on the CPU interrupt pin.

Y-Freeze High Order and Odd/Even Register - Address = FA

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>O/E</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Y-C</td>
<td>Y+F</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

V-F8: This bit is the Y-Freeze high order (MSB) bit
which should be concatenated with the Y-Freeze
Low Order Register contents to form the complete
9-bit Y-Freeze address. As with the Y-Freeze Low
Order Register, this bit is loaded with the value of
the current Y-counter when the FRZ bit = 1 and a
negative transition is detected on the Interrupt Pin.

Y-CB: This is the MSB of the current Y-counter, i.e., the
current line number, and should be concatenated
with the current Y-Freeze Low Order Register to
determine the line number.
4,177,462

O/E: Indicates whether the screen is currently displaying the odd field or even field.
O/E = 0 = Even Field
O/E = 1 = Odd Field

Currently Y Low Order Register - Address = FB

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LSB</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Low order bits of the current Y (line) counter. This counter is reset on the leading edge of V-blank, and incremented by each succeeding H-blank pulse.

READ/WRITE REGISTERS

Each segment to be displayed on the screen has a set of Registers in the composer which are used to describe the coordinates of that segment on the screen and the attributes of the object image or images in such segment. A total of 16 objects can be displayed using one composer. The set of registers for each segment are as follows (the XXXX is used to designate one of the 16 objects):

ROM Pointer Low Order - Address = 0000 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RP7</td>
<td>RP6</td>
<td>RP5</td>
<td>RP4</td>
<td>RP3</td>
<td>RP2</td>
<td>RP1</td>
<td>RP0</td>
<td></td>
</tr>
</tbody>
</table>

RP8-RP7—the low-order eight bits of the first ROM Address containing the segment information.

ROM Pointer High Order and Color - Address = 0001 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RED</td>
<td>GRN</td>
<td>BLU</td>
<td>RP12</td>
<td>RP11</td>
<td>RP10</td>
<td>RP9</td>
<td>RP8</td>
<td></td>
</tr>
</tbody>
</table>

RP8-RP12—the high-order five bits of the first ROM Address containing segment information. These bits are concatenated with the ROM Pointer Low Order bits.

BLU, GRN, RED—bits defining the color of the object image. A "0" means that color is off, a "1" means that color is on.

ΔX, Intensity and X-Copy - 0010 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X-COPY</td>
<td>INT</td>
<td>INT</td>
<td>ΔX4</td>
<td>ΔX3</td>
<td>ΔX2</td>
<td>ΔX1</td>
<td>ΔX0</td>
<td></td>
</tr>
</tbody>
</table>

ΔX0-ΔX4—These five bits specify how many bytes wide the segment is.

INT 1 and INT 0—Specify the intensity of the object in the segment. Four levels of intensity, with 00 being the lowest level and 11 being the brightest.

X-COPY—When this bit equals zero, the ROM pointer is incremented after each byte fetch until ΔX is decremented to zero. When this bit equals one, the ROM pointer is not decremented after each byte fetch (only after the last fetch).

ΔY Register: Address = 0011 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This register indicates the height of the segment or, in other words, how many scan lines include information defining it. For example, if ΔX = 5 and ΔY = 20 for a particular object, then the object is described by a five byte (40 dot) by 20 line (in each field) array in ROM 31.

X-Value Register: 0100 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

X-ORDA0-X-ORDA3—X-order entry for List A.

Y-VAMSB—The most significant bit of the Y-coordinate of the object for List A.

Y Value High Order and X-Order List B - Address = 1000 XXXX

<table>
<thead>
<tr>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y-VB</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>ORD</td>
<td>B3</td>
<td>ORD</td>
<td>B2</td>
<td>ORD</td>
</tr>
</tbody>
</table>

X-ORDB0 through X-ORDB3—X-order entry for List B.

Y-UBMSB—The most significant bit of the Y-coordinate of the object - List B.

The coupler of the invention has been programmed, utilizing the specific register implementation described above, to display a "pinball" video game which is externally controlled by a user. The following pages is program listing of the assembled language for such game.
The microprocessor utilized is the previously mentioned F-8 microprocessor available from Mostek Corporation and the Fairchild Semiconductor Components Group of Fairchild Camera and Instrument Corporation. It was programmed in accordance with the F-8 User's Guide and Guide to Programming available in 1976 from Fairchild; and the 1975 F-8 Preliminary Data Book available from Mostek. The memory allocations (in hexadecimal) for the following are:

ROM "Pinball" Program: F800-FFAF
Display Composer: 0800-OBFF
ROM Segment Information: 1000-17FF

Also, the designation UM1 is used to refer to the display composer; and the designation UM 2 is used to refer collectively to the system controller, the timer and the timing and sync signal generator.
C
0000
0001  *   INITIALIZATION PACKAGE COMMON TO *
0002  *   ALL PROGRAMS ON THE UKI/UMC *
0003  *   SYSTEM PROGRAM PACKAGE REQUIRES *
0004  *   MEMORY LOCATIONS F800 THROUGH *
0005  *   F83F - A TOTAL OF 40 BYTES (HEX) *
0006  *
0007  *
0008  *
0009  *  PROGRAM FUNCTIONS: *
0010  *  (1) CLER LOADS MEMORY LOCATIONS *
0011  *  (2) INIT TRANSFERS MX BYTES OF *
0012  *  DATA <X> BEING STORED *
0013  *  IN REGISTER 1) STARTING *
0014  *  AT LOCATION GIVEN BY *
0015  *  REGISTER 0 TO LOCATION *
0016  *  GIVEN BY REGISTER H. *
0017  *
0018  *
0019  *
0020  *  (3) INTS INITIALIZES ALL UM *
0021  *  REGISTERS WITH DATA *
0022  *  STARTING IN LOCATION *
0023  *  GIVEN BY REGISTER 0 *
0024  *  (4) SYNC SYNCHRONIZES TO LINE *
0025  *  NUMBER HEX D. WILL NOT *
0026  *  SYNCHRONIZE TO CORRECT *
0027  *  FIELD: *
0028  *
0029  *
0030  *
0031  *  PROGRAM ENTRY POINTS: *
0032  *  CLER----H'F800' *
0033  *  INTS----H'F817' *
0034  *  INIT----H'F80D' *
0035  *  SYNC----H'F837' *
0036  *
0037  *
0038  *
0039  *  DP6  H'F800' *
0040  *  F860  PA 00 00 00 CLER  DCI  H'800' *
0041  *  F803  50 90  L1  H'90' *
0042  *  F805  51  LR  1,A  SET COUNTER *
0043  *  F806  30 FF  L1  H'FF' *
0044  *  F808  17  CLR1  ST  1  DECREMENT FF *
0045  *  F809  31  DS  1  STORE FF *
0046  *  F80A  54 FD  BNZ  CLR1  DONE? *
0047  *  F80C  1C  POP  YES--RETURN *
0048  *
0049  *  INIT  LR  DC+0  SET ORIGIN ADDRESS *
0050  *  L1  H'60'  GET CONTENTS SAME *
0051  *  LP  0,DC  SAVE NEW ORIGIN *
0052  *  F810  10  LR  DC+H  SET DEST. ADDRESS *
0053  *  ST  TRANSFER BYTE *
0054  *  F811  17  LP  H+DC  SAVE NEW DEST. *
0055  *  F812  11  SC  1  DECREMENT COUNTER *
0056  *  F813  31  DNZ INIT TRANSFER DONE? *
0057  *  F81C  1C  POP  YES--RETURN *
0058  *
0059  *  INTS  LR  Y,P  SAVE RETURN ADDR. *
0060  *  PI  CLER  CLEAR REGISTERS *
0061  *  LI  H'60'  SET TRANSFER COUNT *
0062  *  LP  1,A  AND STORE IN 1 *
0063  *  F81E  PA 00 00  DCI  H'800' *
0064  *  F821  11  LR  H+DC  SET DEST. ADDRESS *
0065  *  PI  INIT *
0066  *  F835  50 10  LI  H'10' *
0067  *  F837  08  ADC  V.L.C.A LOAD *
0068  *  F828  11  LR  H+DC  TRANSFER COUNT *
0069  *  F829  51  LR  1,A  TRANSFER COUNT *
0070  *  F82A  F8 00 00  PI  INIT *
0071  *  DCI  H'80F0' *
0072  *  F830  11  LR  H+DC *
0073  *  F831  77  L1S  H'7' *
0074  *  F832  51  LR  1,A  TRANSFER COUNT *
0075  *  F833  F8 00 00  PI  INIT SET SELECTED REGS. *
0076  *  PK  AND RETURN
0046 F837 2A 08' FB SYNC DCI H'0BF'
0047 F83A 16 LM GET LINE NUMBER
0048 F836 25 0D CI H'D'
0049 F83B 9F 09 HNZ SYNC ARE WE AT LINE D?
0050 F83F 1C PDP YES--RETURN.
0054 04C X EOU H'0'
0050 04E VV EOU H'1'
0050 04F VV EOU H'2'
0050 050 VV EOU H'3'
0050 05A VYV EOU H'4'
0051 SCOR EOU H'5'
0052 PSTA EOU H'6'
0053 SCAR EOU H'7'
0054 TEMP EOU H'8'
0055 TNP1 EOU H'9'
0056 TNP2 EOU HA
0057 HU EOU H'0'
0058 ML EOU H'1'
0059 DRS H'F900'
005A F900 2A 08 F7 DCI H'0F7'
005B F903 70 CLR CLEAR ACCUMULATOR
005C F904 17 ST DISABLE DMA-VIDEO
005D F905 2A 12 30 DCI H'1200' START INIT. DATA
005F F908 08 LR 0,DC INTO REGISTER 0
005F F909 28 F8 17 PI INTS INITIALIZE REGISTERS
0060 F90C 70 LIS H'0' CLEAR ACC
0061 F90D 55 LR SCRA, A CLEAR SCORE REGISTER
0062 F90E 66 LISU 6
0063 F90F 09 LISU 0
0064 F910 5C LR S,A SET HEX SCORE TO ZERO
0065 F911 64 LISU 4 H'20' * BALL CNTR REGISTER
0066 F912 75 LIS H'5'
0067 F913 5C LR S,A SET FOR FIVE BALLS
0068 F914 6C LISU 4
0069 F915 70 LISU 0
006A F916 5C LR S,A SET INIT. FIN.MOD REG<PRG COPY>
006B F917 63 LOOP LISU 3
006c F918 68 LISU 0
006d F919 28 F8 37 PI SYNC
006E F91C 28 08 FA DCI H'0FA'
006F F91F 70 CLR
0070 F920 8C XM LOOP
0071 F921 91 F5 BM LOOP
0072 F923 20 44 LI H'44' PROPERLY SYNHED
0073 F925 28 08 F7 DCI H'0F7'
0074 F928 17 ST
0075 F929 5C LR S,A SET COMMAND REGISTER
0076 F92A 65 LISU 5
0077 F92B 78 LIS H'8' SET CENTRAL BUMPER
0079 F92C 5C LR S,A
0079 F92D 60 LISU 0
007A F92E 80 OUTS 0 CLEAR BUTTON PORT
007B F92F 20 3A LI H'3A' INIT Y COORD
007C F931 52 LR Y+ A INTO Y
007D F932 20 7E LI H'7E'
007E F934 56 LR X+ A
007F F935 71 LIS H'1'
0080 F936 51 LR Y+ A
0081 F937 70 LIS H'0'
0082 F938 53 LR Y+ A
0083 F939 44 LR VV+ A
0084 F93A 28 F9 8B LP1 PI CN6C CHANGE BACKGROUND TO RED
0085 F93B 00 INC 0 GET INPUT
0086 F93C 94 6C BMZ LP2 IS THERE ANY?
0087 F940 23 F9 A7 PI UPDV NO--UPDATE X COORD
0088 F943 28 F9 96 PI CHSE CHANGE COLOR TO PURPLE
0089 F945 28 8D 1A PI CENE CHECK FOR BUMPER COLOR CHANGE
008A F949 9F F0 BR LP1 AND LOOP BACK
008B F94B 60 LS TEMP A LOAD INPUT IN TEMP
008C F94C 28 F9 97 PI PACK THEN PACK IT
008D F94E 28 F9 6P LP3 PI UDO UPDATE FALLING BALL
008E F952 28 F9 A7 PI DEFY MATCH INACTIVE TO ACTIVE LIST
008F F955 28 F9 BC PI FILL PUT X & Y CURRENT ON LIST
0040 F958 28 FB AC PI SORT SORT INACTIVE LIST
0041 F958 28 F9 96 PI CGSB SYNCHRONIZE SWITCH BACKGROUND
0042 F957 28 FB 1A PI CENS CHECK FOR BUMPER COLOR CHANGE
0043 F941 28 FC 0D PI SCHD UPDATE SCORE
0044 F944 28 FE 3E PI PADC SET PADDLES
0045 F94F 63 LIU 3
0046 F948 68 LILC 0
0047 F969 4C LR AS GET PROGRAM COMREG
0048 F982 82 40 XI H'40' COMPLEMENT A/NUL B
0049 F984 2A 08 F7 DCI H'8F7'
004A F96F 17 ST SA
004B F971 28 F9 BB PI CGSB CHANGE COLOR RED
004C F971 28 FC 8A PI F8H FLASH IF COLLISION
004D F977 A0 INC 0 GET INPUT (IF ANY)
004E F978 94 DE ENZ LP2 IS THERE ANY?
004F F979 70 LIS H'07' NO CLEAR PTA
0050 F979 56 LR PSTK A
0051 F97C 90 DE BR LP3 AND CONTINUE
0052 F976 2A 08 FB CLRS DCI H'8FB'
0053 F981 16 LM GET LINE NUMBER
0054 F982 E5 XR TEMP AT DESIRED LINE?
0055 F983 94 FA ENZ CLRS YES.
0056 F985 28 08 F5 DCI H'8FB' GET NEW BACKGROUND
0057 F988 4A LR A+TMP2 STORE IT
0058 F989 17 ST AND RETURN
0059 F988 08 CGSB LR K+P SAVE RETURN ADDRESS
005A F98C 26 38 LI H'38' BACKGROUND RED
005B F982 59 LR TEMP A
005C F9EF 2A 11 LI H'11' BACKGROUND RED
005D F991 9A CGSB LR TMP2 A
005E F992 28 F9 7E PI CLRS AND RETURN
005F F999 0C PK 
0060 F996 0B CGSB LR K+P LINE FOR CHANGE
0061 F997 78 LIH H'8'
0062 F998 59 LP TEMP A
0063 F999 20 1D LI H'1D' BACKGROUND PURPLE
0064 F99A 2A 0F F5 BR CGSB
0065 F99B 49 DCI H'16' PACK
0066 F99C 12 SP 1
0067 F99F 5A LR TMP2 A BIT 1=PADDLE RIGHT
0068 F9A0 49 LR A+TEMP
0069 F9A1 21 01 NI H'1'
006A F9A8 15 SL 4
006B F9A9 EA XR TEMP2 BIT 0=PADDLE LEFT
006C F9AD 26 LI PTA A STORE PACKED
006D F9AE 1C PDP AND RETURN
006E F9A7 08 UPDX LR K+P SAVE RETURN ADDRESS
006F F9AB 40 LR A+X
0070 F9AB 11 AS VX
0071 F9A4 26 KO LR X A
0072 F9A5 25 5C CGI D'S2'
0073 F9A6 20 07 ENC UPD2 AT LEFT ENDUP?
0074 F9A9 28 FC AS1 P1 VCH YES.
0075 F9F7 24 F9 D1 JMP FL3
0076 F9F7 2A 0A UPD2 CI D'S16'
0077 F9F7 92 F7 ENC UPD1 AT AT ENDUP?
0078 F9F9 29 F9 D1 JMP FL3 NO.RESET X AND RETURN
0079 F9FB 08 FILL LR K+P SAVE RETURN
007A F9F0 28 FB 98 PI PREP
007B F9F1 7F LR FL1 DC0
007C F9F2 16 LM
007D F9F2 25 0F CI H'F' SAVE X ORDER POINTER
007E F9F4 2C XDC LR DC+H GET Y L.O.PTR
007F F9F5 16 LR LM INCREMENT IT
0080 F9F7 84 06 B2 FL2 YES.
0081 F9F9 11 LR H+DC NO.UPDATE X=O
0082 F9FA 2C XDC LR 0+DC
0083 F9FB 0E LR FL1 Y L.O. BALL PTR
0084 F9FC 42 LR A+Y
0085 F9FD 17 ST UPDATE Y
0086 F9FE 40 FL3 LR A+X
0087 F9FF 2A 08 4F DCI H'84F'
000D F905 17 ST UPDATE X
000E F906 0C PK AND RETURN
000F F907 0B DSPY LR K:P
0010 F908 28 FB 29 PI ACT ACTIVE IN O, INACTIVE IN H
0011 F909 41 LR A:V:Y GET V:Y
0012 F90C 58 LR @:A SAVE IN REG 8
0013 F90D 24 10 LI H:10'
0014 F90E 51 LR I:A SET TRANSFER COUNT
0015 F90F 28 F8 0D PI INIT TRANSFER
0016 F913 20 10 LI H:10'
0017 F915 10 LR DC:0
0018 F916 0E ADC
0019 F917 11 LR H:DC WORD INACTIVE PNTR
001A F918 0F LR DC:0
001B F918 0E ADC
001C F91B 51 LR O:DC WORD ACTIVE PNTR
001D F920 1A TRANSFER COUNT
001E F921 28 F8 0D PI INIT TRANSFER
001F F925 48 LP A:B GET V:Y
0020 F929 51 LR V:Y:A RESTORE IT
0021 F92C 0C PK AND RETURN
0022 F92D 08 UD0 LR K:P SET ADDRESS FOR RETURN
0023 F92E 0B D3 LIU 2
0024 F92F 68 LIIS 0 SET ISAR FOR DBC OFFSETS
0025 FA55 44 UD LR A:V:YP GET L.O. BITS FOR V:Y
0026 FA56 24 01 AI H:1’ ADD ACCELERATION
0027 FA58 54 LP V:YP:A SAVE RESULTS
0028 FA5F 92 06 BNC V:DP IF CARRY: MUST INCR. H.O. VY BIT
0029 FA6B 48 LR A:VY
002A FA6C 24 10 AI H:10'
002B FA6E 90 07 BR UD2
002C FA6F 14 UD1 SP 4
002D FA70 59 LR TEMPA:V SAVE NEW VY LO BITS
002E FA72 45 0A LR A:VY GET VY
002F FA73 21 F0 NI H:FO’ CLEAR ALL SAVE H.O.BITS
0100 FA75 09 AS TEMP AND CALCULATE NEW VY
0101 FA76 53 UD2 LR VY:A SAVE RESULT AND
0102 FA77 0A AS Y UPDATE THE Y COORD.
0103 FA78 50 CI H:38’
0104 FA79 92 07 BNC UD5 ABOVE TDP BOUNDARY?
0105 FA7C 2B 39 LI H:39’ YES.
0106 FA80 52 LR V:A SET NEW Y,
0107 FA82 29 FC 9E JMP VYCH COMPLEMENT VY & RETURN
0108 FA81 25 F0 UD3 CI H:FO’ BELOW BOTTOM BOUNDARY?
0109 FA84 82 04 EC UD4
010A FA86 29 FC 2D JMP RSET RESET OR END GAME
010B FA88 52 UD4 LR Y:A NO. SAVE Y COORD.
010C FA8A 40 LR A:X GET X COORD.
010D FA8C 18 CI H:09’ UPDATE IT
010E FA8C 5C LP X:A AND STORE IT
010F FA8E 25 15 CI H:15’
0110 FA91 09 0E BNC UD6 OFF LEFT BOUNDARY?
0111 FA94 26 16 LI H:16’ YES.
0112 FA95 58 LR X:A
0113 FA98 26 FC A5 PI VYCH COMPLEMENT VX
0114 FA99 90 08 BR UD6
0115 FA9A 38 DF UD5 CI H:DF’
0116 FA9B 25 07 BC UD6 OFF RT BNDARY?
0117 FA9C 26 FC A5 LI H:DE’ YES
0118 FA9D 50 LR X:A
0119 FA9F 30 28 FC A5 PI VXCH
011A FAAC 48 UD6 LP A:Y SET Y COORD
011B FA9B 35 75 CI D:97’ Y.G.T. 117?
011C FA9D 2E 35 BNC EDRT:2 NO--POSSIBLE OBJ 8-11 COLLISIONS
011D FA9E 29 48 UD7 CI D:75’ Y.E. 76?
011E FA9F 26 23 BC UDRT Y.E. 97?
011F FAAD 25 0C UD8 CI D:92’ NO. POSSIBLE COLLISIONS
0120 FAAB 25 20 BC UD6 Y.G.T. 92?
0121 FAAC 25 63 CI D:99’ YES.
0122 FAAD 82 1B BC UDRT Y.G.T. 92 & Y.E. 100?
0123 FA44 73 UD9 LIS H:3’ NO. CAN HAVE COLLISION
0124 FA45 59 LR TEMP:A SET POSSIBLE SCORE ADD
0125 FA46 70 CLR CLEAR ACCUMULATOR
0126 FA48 70 X GET X WITH STATUS IN
0127 FA48 2A 6B 2F BWC HI:DE’ SET DCO FOR OBJ 8 CHECK
0128 FA48 81 04 BP UD8 CHECK OBJ 11? INSTEAD?
0129 FA4D 26 98 LI H:98’ YEST. SET X COORD OFFSET
012A FA4F 8E , UDA ADC
0128 FAS9 0E UDB LR O,DC OLYX COORD, OUXY COORD
012C FAS1 20 12 LI H'12', X OFFSET FOR RT COL.
0130 FAS5 5D LR 1:A STORE IN SCRATCH 20(OCTAL).
013E FAS4 7A LIS H'A' Y OFFSET FOR BOTTOM COLLIS.
013F FAS5 5E LR D:A ST. IN SCR 21 & RESET ISAR.
0130 FAS6 28 FC 5A PI TBLCL CHECK FOR COLLISION.
0131 + CHECK FOR POSSIBLE CENTRAL BUMPER COLLISION.
0132
0133 FAS9 42 LR A'Y' GET Y COORDINATE.
0134 FAS5 25 73 CI D'115' TOPSIDE DANGER POINT.
0135 FAS6 92 12 BNC UDK CHECK IF Y>115.
0136
0137 FAS5 0C UDR PK LIS H'8' DONE, SD RETURN.
0139 FAS6 5F UDC LIS H'8' SET POSSIBLE SCORE ADD.
013A FAS6 70 CLR X GET X WITH STATUS IN.
013B FAS5 60 X X.
013C FAS7 5A 53 47 DCI H'S347' SET DCO FOR OBJ 9.
013D FAS6 81 E9 BP UDB CHECK OBJ 10 INSTEAD.
013E FAS8 20 6A LI H'6A' YES, SET OFFSET.
013F FAS6 90 E4 EDPT BR UDA AND GD ADD IT IN.
0140 FAS6 29 FA 6F JMP UDK.
0141 FAS6 42 UDK LR A'Y' GET Y COORDINATE.
0142 FAS7 25 89 CI D'137' BOTTOMSIDE CENTER BUMP DANGER PT.
0143 FAS7 92 15 RNC UDO CHECK OBJ 13?
0144 FAS7 70 LIS H'0' YES, SET POSSIBLE.
0145 FAS7 59 LR TEMPA SET POSSIBLE SCORE ADD.
0146 FAS7 26 7B 79 DCI H'878' SET X&Y COORDS, TEST OBJECT.
0147 FAS9 60 0A 5 DCI OLYX COORD.
0148 FAS7 29 12 LI H'12' WIDTH OF TEST OBJECT.
0149 FAS7 5D LR I:A INTO SCRATCH 20(OCTAL).
014A FAS7 7E LIS H'E' WEIGHT OF TEST OBJECT.
014B FAS7 5E LR D:A INTO SCRATCH 21.
014C FAS7 28 FC 5A PL TBLCL CHECK ON COLLISION.
014D + CHECK FOR POSSIBLE LOWER BUMPER COLLISIONS...
014E + NECESSARY IF THE BALL IS STRADDLING BOTH THE
014F + CENTRAL BUMPER LOWSIDE DANGER POINT, AND THE
0150 + HIGHSIDE DANGER POINT OF THE TOP TWO OF THE BOTTOM
0151 + BUMPER.
0152
0153 FAS2 42 LR A'Y' GET Y COORDINATE.
0154 FAS3 25 88 CI D'136' HIGHSIDE DANGER POINT, LOW BUMPERS.
0155 FAS5 9E 02 BNC UDI IF Y>136, MUST CHECK.
0156
0157 FAS7 0C PK AND RETURN.
0158 FAS8 71 UD10 LIS H'1'.
0159 FAS9 59 LR TEMPA SET POSSIBLE SCORE ADD.
015A FASA 20 1A LI H'1A' WIDTH AND HEIGHT OF BUMPERS.
015B FAS8 5D LR I:A STORE IN SCRATCH 20(OCTAL).
015C FAS7 5E LR D:A AND 21(OCTAL) & RESET ISAR.
015D FAS8 4E 48 AY GET Y COORD.
0156 FAS7 26 A7 CI D'167'.
015F FAS1 92 15 BNC UDI Y.LE. 167?
0160 FAS7 2A 8F 13 UDLO DCI H'8F13' YES, SET FOR OBJ & 2 CHECK.
0161 FAS7 60 CLR CLEAR ACC.
0162 FAS7 5F X YES, SET X WITH STATUS.
0163 FAS8 81 04 BP UDI CHECK OBJ 7 INSTEAD.
0164 FAS8 20 C4 LI H'04' YES.
0165 FASC 8E BNC UDI.
0166 FAS5 0E UD11 LR O,DC OLYX, OUXY COORDS OF BUMPER.
0167 FAS7 26 5A PI TBLCL CHECK FOR COLLISION.
0168 FAS1 48 LI A'Y'.
0169 FAS2 25 A0 CI D'160' Y.LE. 160?
016A FAS4 92 02 BNC UDI Y.LE. 160?
016B FAS6 0C PK YES, NO OTHER COLLISIONS POSSIBLE.
016D FAS8 92 1E BNC UDI Y.LE. 191?
016E FAS8 2A A7 2B UD1 DCI H'722' YES, SET FOR OBJ 3.
016F FAS7 70 CLR CLEAR ACC.
0170 FAS9 5E 0A YS X YES, X IN WITH STATUS.
0171 FAS9 81 04 BP UDI CHECK OBJECT 6 INSTEAD.
0172 FAS2 20 9A LI H'94' YES.
0173 FAS4 8E ABC.
0174 FAS5 0E UD13 LR A,DC.
0175 FAS6 28 FC 5A PI TBLCL CHECK FOR COLLISION.
0176 FAS5 40 LR A'X'.
0177 FAS8 25 2B CI D'43' IF X.LE. 43, RECHECK FOR.
0178 FAS6 82 16 BNC UD10 POSSIBLE OBJ & COLLISION.
0179 FAEE 25 D0  CI D"208" IF X G.T. 208, RECHECK FOR
017A FACC 92 D2  BNC UD10 POSSIBLE OBJ 7 COLLISION
017B FACC 42  LR AY
017C FACC 25 B7  CI H"B7"
017D FACC 92 02  BNC UD14 Y L.E. H"B8"=D"184"?
017E FACC 0C  PK YES; SD NO COLLISIONS LEFT.
017F FACC 25 D7  UD14 CI D"215" CHECK OBJ 455
0180 FACC 92 18  BNC UDEP=42 IF Y G.T. 215, ONLY PADDLE CAN HIT
0181 FACC 2A BP 43  DCI H"BP43" SET FOR OBJECT 4
0182 FACC 70  CLR CLEAR ACC
0183 FADD 0 E0  XS X GET X IN WITH STATUS
0184 FADD 81 04  SP UD15 CHECK OBJ 5 INSTEAD?
0185 FADD 2E 64  LI H"64" YES
0186 FADD 0E 8E  MBC ABC
0187 FADD 06 0E  UD15 LR A0 DC
0188 FADD 28 FC 5A  PI TBCD CHECK FOR COLLISION
0189 FADD 40  LR A5 X
018A FADD 25 43  CI D"62" Y L.E. 62? IF SD, RECHECK FOR
018B FADD 02 C0  BC UD1 POSSIBLE OBJ 3 COLLISION
018C FADD 25 28  CI D"184" IF X G.T. 184, RECHECK FOR
018D FADD 92 C9  UDEP BNC UD1 POSSIBLE OBJECT 6 COLLISION
018E FADD 29 FA E6  JMP UD5
018F FADD 42 UD5 LR AY GET Y Coord
0190 FADD 25 D0  CI H"ID"
0191 FADD 82 2A  BC PPUUP Y"H"ID"?
0192 FADD 25 EC  CI H"EC" YES.
0193 FADD 92 26  BNC PPUUP Y L.E. H"EC"?
0194 FADD 28 FB 15  PI UPAK UNPACK PADDLE STATUS
0195 FADD 02 C9 57  DCI H"29A" SET FOR OBJ 12 CLEAR
0196 FADD 2B FB 22  PI STA1 SET WIDTH FOR STATUS=1
0197 FADD 70  CLR CLEAR ACCUMULATOR
0198 FADD 0E  XS X X Coord IN WITH STATUS
0199 FADD 81 0F  SP UDPS CHECK OBJ 14 INSTEAD?
019A FADD 20 3C  LI H"3C" YES.
019B FADD 8E  MBC RST X Coord FOR STATUS=0
019C FADD 70  CLR CLEAR ACCUMULATOR
019D FADD 0E  XS TMP3 GET STATUS OF OBJ 14
019E FADD 94 0C  BNZ UDPS STATUS=0?
019F FADD 7B 06  LIC H"8" YES.
01A0 FADD 8E  MBC RST X Coord FOR STATUS=0
01A1 FADD 25 FB 2D UDPS PI STA0 RST XCoord FOR STATUS 0
01A2 FADD 9C 05  BR UDPS
01A3 FADD 70  UDPS CLR CLEAR ACC
01A4 FADD 8A  XS TMP2 GET STATUS OF OBJ 12
01A5 FADD 2C 36  FG UDPS IF STATUS=0;RESET WIDTH
01A6 FADD 70  UDPS LIR H"0".
01A7 FADD 59  LR TEMPA; SET POSSIBLE SCORE ADD.
01A8 FADD 0E  LR C 0=DC QU=X Coord, QL=Y Coord
01A9 FADD 0E  XS FD5A PI TBCD CHECK FOR COLLISION
01AA FB34 0C  PPUUP PK AND RETURN
01AB FB15 46  UPAK LR A+PSTA
01AC FB16 14  SR 4
01AD FB17 0A  LR TMP2;A
01AE FB18 46  LR A+PSTA
01AF FB19 21 01  NI H"1"
01B0 FB1B 5B  LR TMP3;A
01B1 FB1C 1C  POP
01B2 FB1D 20 10  STA0 LI H"10" STATUS 0 WIDTH
01B3 FB1F 5D  LR I;A IN SCRATCH 20
01B4 FB20 90 04  BR STA2
01B5 FB22 20 18  STA1 LI H"18" STATUS 1 WIDTH
01B6 FB24 5D  LR I;A IN SCRATCH 20
01B7 FB25 20 14  STA2 LI H"14" HEIGHT IN EITHER STATUS
01B8 FB27 5A  LR D+ A INTO 21 AND RESET ISAR
01B9 FB28 1C  POP RETURN
01BA FB29 0A 08 50 ACT DCI H"50"
01BB FB2C 11  LR H;DC
01BC FB2D 63  LISU 3
01BD FB2E 68  LISL 0
01BE FBBF 42  LR A+S GET PROG COHREG
01BF FB30 18  DCI COMM
01C0 FB31 21 40  NI H"40"
01C1 FB33 12  SR 1
01C2 FB34 12  SR 1
01C3 FB35 8E  MBC Y L.O.ACTIVE ADDR
01C4 F396 0E  LR 0+DC  STORE IN REG 0
01C5 F337 10  CON
01C6 F399 21 10  MI H'10'
01C7 F33A 10  LR DC\H
01C8 F3B6 8E  ADC Y L.O. INACTIVE ADDP
01C9 F3C1 11  LR H+DC STORE IN REG H
01C8 F3DE 08  PADP AND RETURN
01CD F3E0 00  K+P SAVE RETURN ADDR FEEDS
01CE F3F8 8B  PI UPACK UNPACK PADDLE STATUS
01CF F3F9 70  CLR CLEAR ACCUMULATOR
01D0 F3FA EA  X5S TMP2 LEFT PADDLE STATUS IN
01D0 F3FA EA  X5S TMP2 LEFT PADDLE STATUS IN
01D0 F3DB 8F 2F 7E  PI STO NO.
01D1 F3EC 2F F8 87 PAD2 PI UDFP UPDATE LEFT PADDLE PNTP
01D2 F3EC 2F F8 7E  PI ST1 ASSUME RT PAD STATUS=1
01D3 F3EF 20 2A  LI H'2A'
01D4 F3E1 08  CS 0
01D5 F3E2 58  LR 8+A OFFSET ADDRESS FOR RT PAD IMAGE
01D6 F3E3 70  CLR CLEAR ACCUMULATOR
01D7 F3E4 EB  XR SMP3 RT PAD STATUS IN
01D8 F3E5 84 17  ENZ PAD5 STATUS REALLY=1?
01D9 F3E5 20 2A 49  DCI H'849' NO. SET X Coord
01DA F3E5 20 10  LI H'AA' OF RIGHT PADDLE
01DB F3E5 1F 7E  SM ACCORDINGLY
01DC F3E5 20 2A 75  PI ST0 SET POINTERS FOR STATUS=0
01DD F3E6 20 2A  LI H'2A'
01DE F3E6 C8  AS 0
01DF F3E7 98  LR 8+A AND OFFSET FOR RT PAD IMAGE
01E0 F3E8 28 F8 8C PAD3 PI UDFP UPDATE RT PADDLE PNTS
01E1 F3E8 4C  PK AND RETURN
01E2 F3E9 28 F8 7E PAD4 PI ST1
01E3 F3E9 20 20  LI H'17'
01E4 F3EA 2A 2A 49  DCI H'849' SET X Coord OF
01E5 F3EA 20 10  LI H'AA' RT PAD STATUS
01E6 F3EA 1F 17  ST ONE MODE
01E7 F3EA 20 20  LI H'17'
01E8 F3ED 20 20  LI 8+A
01E9 F3F3 4B 62  LI H'62'
01EA F3F3 59  LI TEMP+R
01EB F3F3 78  LI H'8'
01EC F3F4 78  LI H'0'
01ED F3F5 5A  LR TEMP+R
01EE F3F5 1C  POP
01EF F3F6 20 17  ST1 LI H'17'
01F0 F3F7 78  60  LR 8+A
01F1 F3F8 29 62  LI H'62'
01F2 F3F8 59  LR TEMP+R
01F3 F3F9 78  LI H'0'
01F4 F3FA 5A  LR TEMP+R
01F5 F3FB 10  POP
01F6 F3FC 00 07  UDPL DCI H'807'
01F7 F3FD 90 04  BR UDPP
01F8 F3FE 2A 00 07 UDPP DCI H'807'
01F9 F3FF 48  UDPP LR A+8
01FA F400 17  ST
01FB F401 1F  LI H'1F'
01FC F402 8E  ADC
01FD F404 49  LR A+TEMP
01FE F405 17  ST
01FF F406 7F  LIS H'7F'
0200 F407 8E  ADC
0201 F408 4A  LR A+TMP2
0202 F409 17  ST
0203 F40A 1C  POP
0204 F40B 2A 00 50 PREP DCI H'850'
0205 F40C 63  LISU 3
0206 F40D 68  LISL A
0207 F40E 4C  LR A+R SET PROG COMREG
0208 F40F 21 40  MI H'40' EXTRACT A\HULL B BIT
0209 F411 12  SR 1 0 NOW HAVE OFFSET TO INACTIVE LIST
020A F412 12  SR 1 0 NOW HAVE OFFSET TO INACTIVE LIST
020B F413 11  XL R+H DC TO Y L.O. INACTIVE
020C F414 20  LI H'20' AND SAVE IN H
020D F415 20 20  ADC DC TO Y H.O.+X CIDEP INACTIVE
020F FB9A 0E  LR  0, DC
0210 FB9B 1C  POP
0211 FB9C 08  2DRT  LR  K,P  SET ADDRESS FOR RETURN
0212 FBAD 28  FB 9B  PI  PREP
0213 FBBA 10  SRT1  LR  DC+H  Y L.D.
0214 FBB1 2C  XDC
0215 FBB2 10  LR  DC+0  X ORDER
0216 FBB3 20 10  LI  H'10'
0217 FBB5 59  LR  TEMP,A  SET COUNTER
0218 FBB6 39  SRT2  DS  TEMP  DECREMENT COUNTER
0219 FBB7 16  LM  GET NEXT OBJ NUMBER
021A FBB8 25 0F  CI  H'F'  COMPARE WITH BALL'S OBJ. NO.
021B FBB9 20  XDC
021C FBBB 16  LM  INCRR. H'RESTORE
021D FBBB 2C  XDC
021E FBBF 94  FB  BHZ  SRT2  OBJ=BALL'S?
021F FBBF 0E  LR  0,DC  YES,DCD=1 PAST XORD BALL
0220 FBC0 2C  XDC
0221 FBC1 11  LR  H, DC AND H=1 PAST Y L.D. BALL
0222 FBC2 48  LR  A+HL  GET HL
0223 FBC3 24  FE  AL  H'FE'  H=1 BEFORE Y L.D. BALL NOW
0224 FBC5 5B  LR  H,L, A  H=1 BEFORE Y L.D. BALL NOW
0225 FBC6 49  LR  A, TEMP  GET COUNTER
0226 FBC7 25 0F  CI  H'F'  BALL LOWEST ON LIST?
0227 FBC9 84  3C  BZ  SRT5  BALL LOWEST ON LIST?
0228 FBCB 03  LR  A+OL  NO, GET L.D.BITS OF XORDER ADDR.
0229 FBCC 24  FE  AI  H'FE'  H=1 BEFORE Y L.D. BALL NOW
022A FBCD 07  LR  OL+A  NOW POINTS 1 BEFORE XORD BALL
022B FBCF 0F  LR  DC+0  LOAD DCD
022C FBDO 16  LM  H'S40'
022D FBD1 2A  08  40  DCD  GET OBJ+, PRECEDEING OBJ ON LIST
022E FBD4 0E  ABC  DCD TO X,COORD, THIS OBJECT
022F FBD5 16  LM  NOW HAS ITS X,COORD
0230 FBD6 18  CDM
0231 FBD7 1F  INC  X
0232 FBD8 C0  AS  X
0233 FBD9 92  1A  BNC  EXC1  IF X,BALL<XOBJ, EXCHANGE BACK
0234 FBDA 70  CLR  CLEAR ACCUMULATOR
0235 FBDC E9  XS  TEMP COUNTER IN WITH STATUS
0236 FBD0 84 12  BZ  SRTD  IF BALL HIGHEST ON LIST--DONE.
0237 FBDF 0F  SRT3  LR  DC+0  DCD POINTS TO OBJ+ PREC. BALL
0238 FBEE 16  LM
0239 FBE1 0E  LR  0, DC  0 POINTS TO XORDER BALL
023A FBE2 16  SRT4  LM  GET OBJ+, FOLLOWING BALL
023B FBE3 16  LM  H'S40'
023C FBE4 2A  08  40  DCD  AND DCD POINTS TO ITS X,COORD
023D FBE7 0E  ABC  GET IT
023E FBE8 16  LM  TEMP,A  SAVE IT
023F FBE9 59  LR  A+X  GET X BALL
0240 FBEA 40  LM
0241 FBEB 18  COM
0242 FBEF 1F  INC
0243 FEE9 C9  AS  TEMP
0244 FEE2 92 02  BNC  EXC2  IF XOBJ<X,BALL, EXCHANGE FORWARD
0245 FBF0 0C  SRTD  PK  OTHERWISE, RETURN
0246 FBF1 48  EXC2  LR  A+HL  GET HL
0247 FBF2 1F  INC  INCREMENT IT
0248 FBF3 5B  LR  HL,A  AND STORE
0249 FBF4 2B FB FD EXC1  PI  SWIT  SWITCH X ORDERS
024A FBFF 10  LR  DC+H  0, DC
024B FBFF 0E  LR  SWIT  SWITCH Y L.D.
024C FBFF 28 FB FD  PK  AND RETURN
024D FBFD 0C  LR  DC+0  GET START ADDRESS
024E FBFF 16  LM  AND CONTENTS SAME
024F FBFF 59  LR  TEMP,A  STORE TEMPORARILY
0250 FBFF 16  LM  GET NEXT ITEM
0251 FC00 16  LM  DC+0  STORE IT IN 1ST ADDR
0252 FC01 0F  LR  A,TEMP
0253 FC02 17  ST
0254 FC03 49  LR  A+OL  COMPLETE SWITCH
0255 FC04 17  ST  AND RETURN
0256 FC05 1C  POP
0257 FC06 03  SRTS  LR  A+OL
0259 FC08 24  FF  LR  DL+A  0 POINTS TO XORD BALL
4,177,462

025A FC0A 0F  LR  DC+0  AS DOES DC0
025B FC0B 06  BR  SRT4
025C FC0C 08  SCHD  LR  K+P  SAVE RETURN ADDRESS
025D FC0D 70  CLR  CLEAR ACCUMULATOR
025E FC0E 87  VC  SCRD  GET SCORE ADD WITH STATUS
025F FC10 94  BZ  SCND  HW CHANGE?
0260 FC11 84 66  AI  H'66'  YES
0261 FC12 D5  ASO  SCDR  CALC. NEW DECIMAL SCORE
0262 FC13 55  LR  SCDR+A  AND UPDATE SCORE REG.
0263 FC14 66  LISU  6
0264 FC15 68  LISC  0
0265 FC16 47  LR  A+SCAD  GET SCORE ADD
0266 FC17 CC  AS  S  ADD PREVIOUS HEX SCORE
0267 FC18 5C  LP  S+A  AND UPDATE HEX SCORE
0268 FC19 65  CI  H'65'  
0269 FC1A 60  BC  SCH1  SCORE<99 DECIMAL?
026A FC1B 4D  AL  H'AD'  YES; SUBTRACT D'100'
026B FC1C 5C  LR  S+A  AND UPDATE THE HEX SCORE
026C FC1D 64  LISU  4  NEW WE UPDATE FINAL MOD.
026D FC1E 6C  LISC  4
026E FC1F 4C  LR  A+S  GET PROG COPY FINAL MOD REG
026F FC20 1F  INC  1F  INCREMENT COLOR MOD
0270 FC21 1F  INC  1F  INCREMENT PROGRAM COPY
0271 FC22 5C  LR  S+A  UPDATE PROGRAM COPY
0272 FC23 2A 08 F2  DCI  H'8F2'  
0273 FC24 17  ST  AND UPDATE UNI COPY
0274 FC25 45  SCH1  LR  A+SCDR  RECOVER SCORE
0275 FC26 14  SP  A+K  AND UNPACK OBJECT O VALUE
0276 FC27 59  LR  TEMP+A  SAVE IN TEMP
0277 FC28 28 FC 4A  PI  SET  SET NEW OBJ 0 ADDR IN H
0278 FC29 10  LR  DC+H  
0279 FC2A 45  LR  @+DC  TRANSFER TO @ REGISTER
027A FC2B 14  LC  H+SCDR
027B FC2C 15  SL  4
027C FC2D 14  SR  4  UNPACK OBJ 1 VALUE
027D FC2E 59  LR  TEMP+A  SAVE IN TEMP
027E FC2F 28 FC 4A  DCI  H'800'  
027F FC30 03  LR  A+DL  SET NEW L.O. ROM, OBJ0
0280 FC31 17  ST  
0281 FC32 4B  LR  A+HL  SET NEW L.O. ROM, OBJ1
0282 FC33 17  ST  
0283 FC34 0A 08 10  DCI  H'810'  
0284 FC35 02  LR  A+BU  SET NEW H.O. ROM+COLOR, OBJ0
0285 FC36 17  ST  
0286 FC37 4A  LR  A+HU  SET NEW H.O. ROM+COLOR, OBJ1
0287 FC38 17  ST  PK  AND RETURN
0288 FC39 0C  SCND  SET  DCI  H'1500'  
0289 FC3A 15 00 00  DCI  H'F'  START ADDR POP NUMBERS
028A FC3B 7F  LIS  OFFSET BETWEEN NUMBERS
028B FC3C 0E 64 05  BZ  S3  ALREADY HAVE ZERO?
028C FC3D 8E  S2  ADC  ADD OFFSET
028D FC3E 59  DS  TEMP  DECREMENT COUNTER
028E FC3F 5A 4D  BNZ  S2  ADDED ENOUGH OFFSETS?
028F FC40 11  S3  LR  H+DC  YES; NUMBERS READY, LOAD IN H
0290 FC41 4A  LP  A+HU  GET ROM H.O.
0291 FC42 22 E0  DI  H'EO'  TURN ON COLOR BITS
0292 FC43 5A  LP  H+UA  AND STORE RESULT.
0293 FC44 1C  POP  A+OL  AND RETURN
0294 FC45 0B  TBCL  GET X COORD, TEST OBJ.
0295 FC46 1B  COM  
0296 FC47 1F  INC  
0297 FC48 5A  LR  TMP2+A  SAVE ITS NEGATIVE
0298 FC49 40  LR  A+X  GET X COORD, FALL
0299 FC4A 24 07  AI  H'7'  
029A FC4B 6A  AS  TMP2A
029B FC4C 82 02  BC  TBC1  XCOB G.T. X?7?
029C FC4D 1C  POP  YES; NO COLLISION POSSIBLE
029D FC4E 03  TBC1  LR  A+OL  GET X COORD, TEST OBJ.
029E FC4F 0C  AS  S  ACC=XCOB+WIDTH
029F FC50 18  COM  
02A0 FC51 1F  INC  
02A1 FC52 C0  AS  X
02A2 FC53 92 02  BHC  TBC2  XCOB+WIDTH L.E. X?
02A3 FC54 1C  POP  YES; NO COLLISION—RETURN
02A5 FC6D 49 TBC2 LR A,TMP COLLISION!
02A6 FC6E 57 LR SCORDA SET SCORE ADDITION
02A7 FC6F 67 LISU 7 COLLISION FLAG IN SCRATCH 0/70'
02A8 FC70 71 LIS H/'1' SET COLLISION FLAG
02A9 FC71 5C LR S,A VALUE IN
02AA FC72 62 LR T2 2 RESET ISAR
02AB FC73 40 LP A,X
02AC FC74 24 04 AI H#'4'
02AD FC75 CA 05 AS TMP3
02AE FC77 82 08 BC TBC4 XCOB G.T. X+4?
02AF FC79 07 LR A+9L YES, LEFT SIDE COLLISION
02B0 FC7A 24 F7 AI H'F7' X=XCOB=9
02B1 FC7B 50 TBC3 LP X,A
02B2 FC7D 29 FC A5 JMP VXCH VX=Vy&X=0 RETURN FROM THERE
02B3 FC80 03 TBC4 LR A+9L GET X COORD. TEST OBJ
02B4 FC81 CC AS S ACC=XCOB+WIDTH
02B5 FC82 5B LR TMP5+R SAVE THIS TEMPORARILY
02B6 FC83 1B CDM
02B7 FC84 1F INC
02B8 FC85 C0 AS X
02B9 FC86 24 04 AI H#'4'
02BA FC88 92 05 INC TBC5 XCOB+WIDTH L.E. X+4?
02BB FC89 48 LR A,TMP3 YES,RT SIDE COLLISION
02BC FC8A 1F INC X=XCOB+WIDTH+1
02BD FC8C 90 EF BR TBC3
02BE FC8E 70 TBC5 CLR MUST BE TOP OR BOTTOM COLLISION
02BF FC8F 4B AS VX GET VX IN WITH STATUS
02C0 FC90 4D LR A+1 ADVANCE ISAR TO OFFSET FOR BOT. COL.
02C1 FC91 02 LR A+0U GET XCOB
02C2 FC92 81 07 BP TBC7 IF VX<0,BOTTOM;Vy>0,top,
02C3 FC94 CE AS D Y=YCOB+HEIGHT SAME+1,RESET ISAR
02C4 FC95 1F INC
02C5 FC96 52 TBC6 LP Y,A STORE NEW Y VALUE
02C6 FC97 39 FC 9E JMP VXCH VY=Vy&DONE. VXCH RETURNS
02C7 FC99 24 F7 TBC7 AI H'F7' TOP,SO Y=YCOB=9
02C8 FC9C 90 F9 BR TBC6
02C9 FC9E 43 VXCH LR A+Vy
02CA FC9F 18 CDM
02CB FAC0 1F INC
02CC FAC1 53 LR VX,A
02CD FAC2 15 SL 4
02CE FAC3 54 LR VY,A
02CF FAC4 1C PDP
02D0 FAC5 41 VXCH LR A,VX
02D1 FAC6 1B CDM
02D2 FAC7 1F INC
02D3 FAC8 51 LR VX,A
02D4 FAC9 1C PDP
02D5 FACB 70 F21 CLR CLEAR ACCUMULATOR
02D6 FACF 67 LISU 7 ISAR TO COLLISION FLAG
02D7 FACF EC LISR 0 COLLISION FLAG IN M/STATUS
02D9 FACF 70 LIS H/'A'
02DA FCBF 5C LR S,A CLEAR FLAG
02DB FCBO 94 03 BR F1 COLLISION?
02DC FCBO 94 04 BR F2
02DD FCBO 29 FD 00 F1 JMP SOND
02DE FCBO 28 F2 NOP NO-OPS FOR BREAKPOINTS
02DF FCBO 28 F2 NOP FOR DEBUGGING.
02E0 FCBO 28 F2 NOP DELETE LATER.
02E1 FCBE 2E NOP RETURN
02E2 FCBB 2E PDP
02E3 FCBB CC PDP
02E4 FCBC 2B A0 RSET' LII H/'AO'
02E5 FCBD 5B LR TMP3,A SET TIME DELAY ON RESET
02E6 FCF0 28 F9 36 RST1 PI CMSG
02E7 FCF3 28 FD 1A PI CHIB
02E8 FCF6 28 F9 0B PI CMSC
02E9 FCF9 38 BC TMP3
02EA FCF9 94 F5 BNZ RST1 DELAY DONE?
02EB FCFD 2A 08 F7 DCSI H'OF'
02EC FCFD 74 LIS H#'4'
02ED FCFO 17 ST BEFORE DIDDING LIST A
02EE FC01 64 LISU 4
02EF FC02 68 LISL 0
While the invention has been described in detail in connection with a preferred embodiment thereof, it will be apparent to those skilled in the art that many changes or modifications can be made without departing from the spirit of the invention. It is therefore intended that the coverage afforded be limited only by the language of the claims and its equivalent.

I claim:

1. A method of producing sequential frame displays of object images and background on a display surface area which is scanned by a scanning system to produce each of said frame displays, comprising the steps of:
   storing at predetermined locations sets of information respectively defining a plurality of spatial display segments which individually at least partially define an object image associated therewith it may be desired be displayed at some location on said display area during one or more of said sequential frame displays;
   tracking the scan by said scanning system which produces each of said frame displays;
   responding to said step of tracking indicating that said scanning system is approaching a desired spatial location for a selected spatial segment in one of said frame displays by directing delivery to said scanning system at such time of control signals conforming to the stored information set defining said selected spatial display segment;
   calculating for each of said frame displays the time-distance between spatial display segments which are to be sequentially displayed thereon; and
   providing to said scanning system background control signals directing said scanning system to produce said background display between spatial display segments for said calculated time-distance.

2. Apparatus for producing sequential frame displays of object images for a display surface area which is scanned by a scanning system to produce each of said frame displays comprising:
   memory means to store at predetermined locations sets of information respectively defining a plurality of spatial display segments which individually at least partially define an object image associated therewith it may be desired be displayed during one or more of said sequential frame displays;
   means to convert spatial display segment information to corresponding control signals for said scanning system; and
   means to discharge to said converting means information defining spatial display segments selected to appear in a specified frame display, at a rate correlated with the rate at which said scanning system scans said display surface area to produce said specified frame display, which means accepts delivery of said information from said predetermined locations of said memory means at a rate which is not correlated with the rate at which said scanning system scans said display surface area.

3. Apparatus according to claim 2 wherein said information discharging means includes a first in-first out buffer.

4. Apparatus for producing sequential frame displays for a display surface area which is scanned by a scanning system to produce each of said frame displays comprising:
   memory means to store sets of information respectively defining a plurality of spatial display segments which individually at least partially define an object image associated therewith it may be desired be displayed during one or more of said sequential frame displays;
   means to provide information defining a display surface area background for object images to be displayed during a specified frame display;
   means to convert said spatial display segment information and said background information to corresponding control signals for said scanning system;
   means to track the scan by said scanning system which produces said specified frame display;
   means responsive to said scan tracking means indicating that said scanning system is approaching a desired spatial positioning for a selected spatial segment by directing said memory means storing the information set defining said spatial display segment to deliver information defining said segment to said information converting means;
   means to calculate for said scan producing said specified frame display the time-distance between spatial display segments which are to be sequentially displayed in said specified frame display; and
   means responsive to calculation of such a time-distance by directing said background information providing means to deliver to said converting means information defining said background for the time-distance so calculated.

5. Apparatus according to claim 2 further including means connected to the output of said information discharging means for storing information indicating modifications to color or intensity information emanating from said information discharging means.

6. Apparatus according to claim 2 further including memory means to store information defining a size multiplication of a spatial display segment, which means communicates with the output of said information discharging means for delivering said multiplication information thereto.

7. Apparatus according to claim 2 further including means to track the scan by said scanning system which produces each of said frame displays, and memory means communicating with said scan tracking means for storing information indicative of a location being scanned when a freeze command signal is received.
8. Apparatus for producing sequential frame displays for display surface area which is scanned by a scanning system to produce each of said frame displays comprising:

- means to store at predetermined locations sets of information respectively defining a plurality of spatial display segments which individually at least partially define an object image associated therewith it may be desired to be displayed at some location on said display area during one or more of said sequential frame displays;
- associative memory means to list at a location separate and apart from the locations at which said sets of information are stored, the spatial display segments selected to be displayed in a specified frame display, the spatial location desired for each therein, and a color or intensity attribute selected for the object image of each of said specified spatial display segments;
- means to track the scan by said scanning system which produces each of said frame displays;
- means responsive to said tracking means indicating that said scanning system is approaching a desired spatial location for a selected spatial segment in said specified frame display by directing delivery to said scanning system at such time of control signals conforming both to the stored information sets defining said selected spatial display segment and to the selected color or intensity attribute of the object image thereof; and
- means to update as required for a succeeding frame display both the sets of information defining spatial display segment to be displayed and the selected intensity or color attributes thereof.

9. Apparatus according to claim 2 further including first offset memory means to store information indicative of a location in the Y direction on said display surface area at which the first line to be scanned is to be positioned during a specified frame display, and means responsive to said first offset memory means containing information indicative of a first line location different than the normal first line location by adjusting said first line location to correspond to the location indicated in said first offset memory means.

10. Apparatus according to claim 9 further including second offset memory means to store information indicative of a location in the X direction on said display surface area at which all of said lines to be scanned are to first appear, and means responsive to said offset memory means containing information indicative of a starting location for said lines different than the normal line starting location in the X direction by adjusting said starting location to the location indicated in said second offset memory means.

11. Apparatus according to claim 8 further including means to provide information defining a display surface area background for object images to be displayed during a specified frame display, wherein said display surface area is a display screen of a television receiver and said scanning system is the raster scanning system therefore; means are included for generating the timing and synchronization signals required to produce a composite video signal for the scanning system of said television receiver; each of said sets of information defining a spatial display segment includes indicia defining background for an object image also defined by said set of information; and said delivery means is responsive to said background defining information in each of said information sets by directing said background information providing means to provide information defining background to said converting means for conversion of the same to corresponding control signals for said scanning system.

12. Apparatus according to claim 11 wherein said scan tracking means includes a line counter which indicates the line being scanned by said scanning system at any given time, and further includes means for storing information setting forth a scan line to be compared with said line counter for generation of an interrupt signal.

13. A method of producing sequential frame displays of object images for a display surface area which is scanned by a scanning system to produce each of said frame displays, comprising the steps of:

- storing at predetermined locations sets of information respectively defining a plurality of spatial display segments for said scanning system to partially define an object image associated therewith it may be desired to be displayed at some location on said display area during one or more of said sequential frame displays;
- providing means to convert spatial display segment information to corresponding control signals for said scanning system;
- delivering to information discharge means information extracted from said predetermined locations defining the set or sets of spatial display segments selected to appear in a specified frame display in the order in which such information is required by said scanning system to produce said spatial display segments on said display surface during said frame display; and
- discharging said information from said discharge means to said converting means at a rate correlated with the rate at which said scanning system scans said display surface area to produce each of said frame displays.

14. A method according to claim 13 further including the steps of tracking the scan by said scanning system which produces said specified frame display; and responding to said step of tracking indicating that said scanning system is approaching a desired spatial location for a selected spatial segment by directing delivery of the stored information set defining said spatial display segment for discharge of the information therein defining object images at said rate.

15. A method according to claim 13 wherein said means provided to convert said spatial display segment information to corresponding control signals for said scanning system is also capable of converting information defining a display surface area background to control signals for said scanning system to produce background for said display surface area, and further including the steps of:

- providing information defining a background to be produced by said scanning system at locations at which object images are not to be displayed during a specified frame display;
- calculating for each of said frame displays the time-distance between spatial display segments which are to be sequentially displayed thereon; and
- delivering background defining information so calculated to said converting means between the information delivered thereto defining the spatial display segments for which the time-distance of such background was calculated; and
discharging information defining said background to said converting means for the production by said converting means of background control signals for said scanning system for the time-distance so calculated between said spatial display segments.

16. A method of producing sequential frame displays of object images for a display surface area which is scanned by a scanning system to produce each of said frame displays, comprising the steps of:

storing at predetermined locations sets of information respectively defining a plurality of spatial display segments which individually at least partially define an object image associated therewith it may be desired be displayed at some location on said display area during one or more of said sequential frame displays;

specifying which of said spatial display segments are to be displayed during a selected frame display;

specifying for each of said specified spatial display segments, at a location separate and apart from the location at which said sets of information are stored, a color or intensity attribute selected for the object image of said spatial display segment;

tracking the scan by said scanning system which produces each of said frame displays;

responding to said step of tracking indicating that said scanning system is approaching the desired spatial location for a specified spatial segment in said selected frame display by directing delivery to said scanning system at such time of control signals conforming both to the stored information sets defining said specified spatial display segments and to the specified color or intensity attribute of the object image thereof, and

updating as required for a succeeding frame display both the sets of information defining spatial display segments to be displayed and the selected intensity or color attributes thereof.

17. Apparatus according to claim 4 wherein said means to direct delivery of information defining said segment to said information converting means includes means to discharge to said converting means information defining spatial display segments selected to appear in a specified frame display at a rate correlated with the rate at which said scanning system scans said display surface area to produce said specified frame display, which means accepts delivery of said information from said predetermined locations of said memory means at a rate which is not correlated with the rate at which said scanning system scans said display surface area.

18. Apparatus according to claim 4 further including associative memory means to list at a location separate and apart from the locations at which said sets of information are stored, the spatial display segments selected to be displayed in a specified frame display, the spatial location desired for each therein, and a color or intensity attribute selected for the object image of each of said specified spatial display segments.

19. Apparatus according to claim 2 further including means to provide information defining a display surface area background for object images to be displayed during said specified frame display; and wherein each of said sets of information defining a spatial display segment includes information defining background for an object image also defined by said set of information, and said discharging means is responsive to said background defining information in each of said information sets by directing said background information providing means to provide information defining background to said converting means for conversion of the same to corresponding control signals for said scanning system.

20. Apparatus according to claim 2 wherein said display surface area is a display screen of a television receiver and said scanning system is a scanning system therefor; and further including means for generating the timing and synchronization signals required to produce a composite video signal for the scanning system of said television receiver, and means for superimposing a radio frequency carrier signal on said composite video signal to condition the same for application to the antenna input of said television receiver.

21. Apparatus according to claim 8 further including means to communicate with said approach responsive means for selectively directing the same to repeat a direction to said memory means to deliver an information set defining a selected display segment to said information discharging means, whereby said scanning system produces said selected segment a plurality of times adjacent one another on said display surface area.

22. Apparatus according to claim 17 further including associative memory means to list at a location separate and apart from the locations at which said sets of information are stored, the spatial display segments selected to be displayed in a specified frame display, the spatial location desired for each therein, and a color or intensity attribute selected for the object image of each of said specified spatial display segments.

* * * * *